Front End Processes
2008 ITRS

ITRS Public Conference
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Semicon West

2008 FEP ITWG Meeting Participants:

US: J. Butterbaugh, R. Jammy, L. Larson, M. Walden, M. Goldstein, T. Pan, J. Prasad, L. Chang, K. Reinhard

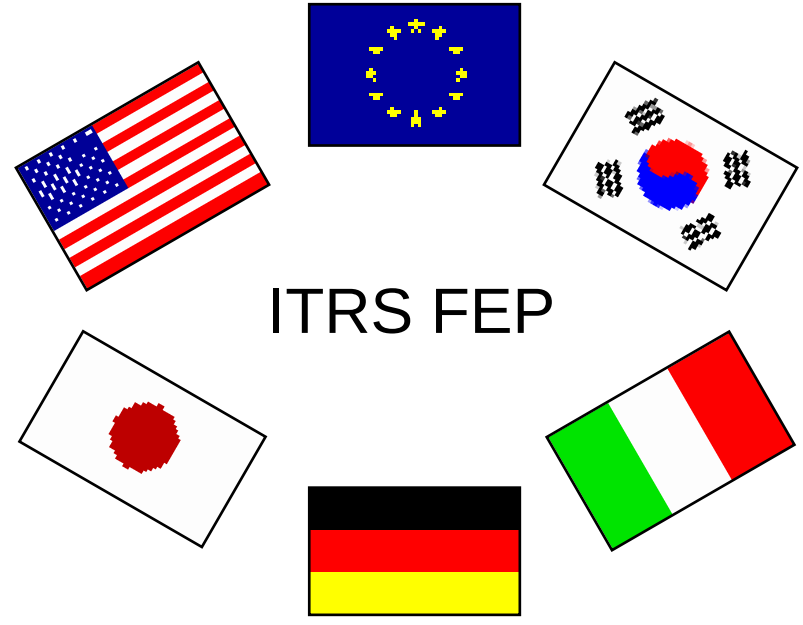
Japan: I. Mizushima, M. Niwa, M. Watanabe, H. Kitajima, J. Cross

Europe: M. Alessandri

Korea: J.S. Roh, D.S. Kil

2008 FEP Sub-TWGs and Chairs

- Starting Materials
  - Mike Walden(US), Mike Goldstein(US)
- Surface Preparation
  - Joel Barnett(US)
- Thermal/Thin Films/Doping
  - Hsing-Huang Tseng(US)
- Etch
  - Greg Smith(US), Gabe Gebara(US)
- Stacked DRAM
  - Jae-Sung Roh(KR)
- Trench DRAM
  - Wolfgang Mueller(EU)
- Flash
  - Mauro Alessandri(EU)
- PCM
  - Mauro Alessandri(EU)
- FeRAM
  - Yoshimasa Horii(JP)



2008 FEP - Highlights

- **Starting Materials:**
  - Incorporate new ORTC scaling for DRAM 2007-2009 and recalculated allowable defects
  - Edge exclusion changed from 1.5mm to 2mm until end of roadmap per Factory Integration
- **Surface Prep:**
  - Particle metrics updated for changes in ORTC DRAM scaling
  - A few clerical corrections
- **Thermal/Thin Films/Doping:**
  - New L_g scaling trend adopted for MPU/ASIC, LOP, and LSTP
  - MPU/ASIC and LSTP: columns shifted and interpolated to adjust for new L_g
  - LSTP: only L_g changed – minor differences from previous scaling model
  - Timing of bulk CMOS, FDSOI, and Multi-gate affected by shift
  - Full remodeling effort for 2009 in collaboration with PIDS
- **Etch:**
  - New L_g scaling trend adopted – absolute variance relaxed – yellow/red 2012/2013
- **Stacked DRAM:**
  - Incorporate new ORTC scaling for DRAM 2007-2009
- **Trench DRAM:**
  - discontinued scaling after 58nm generation in 2008
- **Non-volatile memories**
  - Flash – update potential solutions, high-k need pushed beyond 32nm
  - PCRAM – heater material requirements updated
  - FeRAM – a few corrections; consistency with PIDS; add missing potential solutions figure

Starting Materials
2008 Highlights

- Modified DRAM ½ Pitch and DRAM Total Chip Area consistent with ORTC direction
- This resulted in DRAM Active Transistor Area modification for 2007 – 2009 and affected DRAM Epitaxial and SOI defect density calculations as well as Particles (#/wf) and Particle Density (cm^{-2}) for those same years
- Modified edge exclusion to 2mm (from 1.5mm from 2012 onward) for consistency with FI
- Recalculated affected table entries – slight change in Particle (#/wf) from 2012 onward
- Modified MPU Physical Gate Length (nm) per ORTC direction
- Addressed near-term colorization violations for the 2008 update

Starting Materials
Ongoing Activities

- Reassess MPU-related model impact resulting from loosening of MPU Physical Gate Length and update calculations / colorizations as necessary
- ERO and edge bevel – assessment of SEMI-related activities and potential of model-based table entries (dependency – model availability)
- Edge and backside particles – continued cross-TWG interaction with Surface Prep to understand their efforts and to assess whether there are implications on Starting Materials
- Timing for 450mm remains 2012 in the ITRS – continue to monitor industry activities and assess effect on tables
- Continue consideration of adding emerging materials related line entries into the Starting Materials tables

Surface Preparation
2008 Highlights

- **Particle metrics updated for changes in DRAM models**
- **Minor corrections made to particle metrics**

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	***68***	***59***	***52***	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	***68***	***59***	***52***	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	**32**	**29**	**27**	**24**	**22**	**20**	**18**
Killer defect density, D_pR_p (#/cm^2) [A]	**0.019**	**0.025**	**0.033**	**0.022**	**0.027**	**0.034**	**0.022**
Critical particle diameter, d_c (nm) [B]	**34.1**	**29.7**	**25.8**	**22.5**	**20.0**	**17.9**	**15.9**
Critical particle count, D_{pw} (#/wafer) [C]	**65.1**	**65.1**	**65.1**	**65.1**	**65.1**	**269.4**	**169.7**

Surface Preparation
Ongoing Activities

- Materials loss specs (including high-k/metal gate) to be updated in 2009
- Research targeted on SOI Metal contamination issues
  - New specs to be outlined by Leti when results are available
- Potential Solutions Required
  - Surface passivation for Germanium, SiGe, and III-V
  - Si / SiO_2 loss requirements
  - New material loss requirements
  - Advanced particle removal without damage
  - Pore sealing and the direction to go
  - BEOL material compatibility
  - "Green" chemistry and processing

Thermal/Thin Films/Doping/Etch
2008 Highlights

- New ORTC MPU/ASIC L_g scaling included by shift/interpolation
  - pushes bulk solutions out to 2016 (previously 2012)
  - shifts FDSOI solutions to 2013-2019 (previously 2010-2015)
  - shifts Multigate solutions to 2015-2022 (previously 2011-2022)
  - creates “hole” for metal gate parameters 2008-2010
  - creates “hole” for STI parameters for 2013-2016
- New ORTC LOP L_g scaling included by shift/interpolation
  - pushes bulk solutions out to 2013 (previously 2012)
  - shifts FDSOI solutions to 2013-2018 (previously 2011-2016)
  - shifts Multigate solutions to 2013-2022 (previously 2011-2022)
- New ORTC LSTP L_g scaling included – no changes in parameters

Shift/Interpolate Using L_g – Bulk MPU

some columns shift; interpolate the rest using L_g

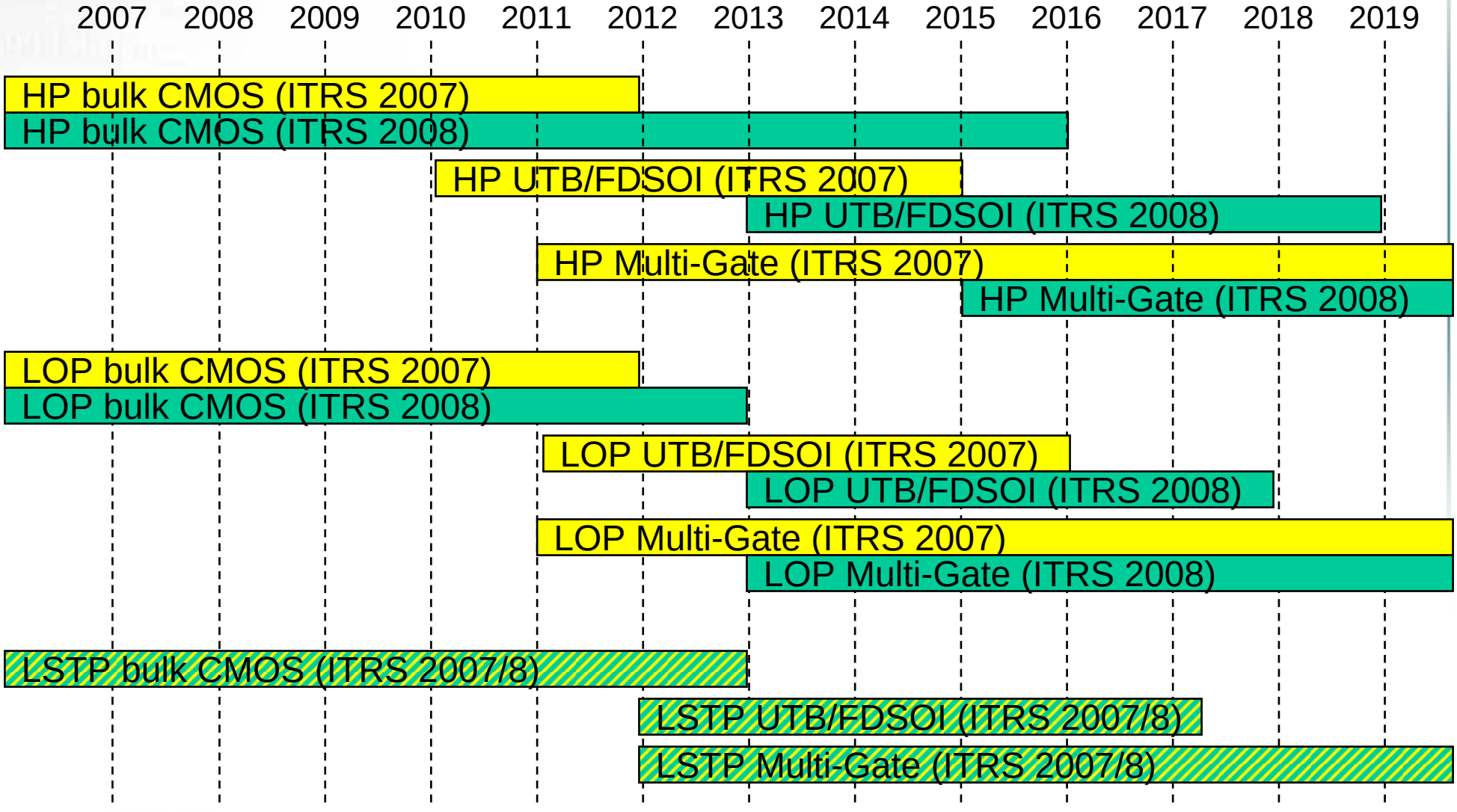
Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
2007 MPU/ASIC Lg (nm)	25	23	20	18	16	14	13	11	10	9	8	7	6.3	5.6	5	4.5
2008 MPU/ASIC Lg (nm)	32	29	27	24	22	20	18	17	15	14.0	12.8	11.7	10.7	9.7	8.9	8.1
Shift/Interpolate Formua	2005	intrp	intrp	intrp	intrp	2009	2010	intrp	intrp	2012	intrp	intrp	intrp	intrp	intrp	intrp
EOT w/3E20 poly, bulk MPU (nm)	1.2	0.71	0.54	0.41												
EOT w/3E20 poly, bulk MPU (nm)	1.3	1.2	1.2	1	0.68	0.54	0.41									
EOT w/metal gate, bulk MPU (nm)		0.9	0.75	0.65	0.55	0.50										
EOT w/metal gate, bulk MPU (nm)			1.0	0.95	0.88	0.75	0.65	0.60	0.53	0.5						
Drain Ext. X_j bulk MPU (nm)	12.5	11	10	9		7										
Drain Ext. X_j bulk MPU (nm)	11	11	11	11	11		9	8.5	7.7	7						

non-steady trend corrected

filled in for metal gate EOT for 2009/10 based on latest conference presentations

Timing of CMOS Innovations

"artifacts of shift/interpolation"



To be addressed in 2009 ITRS

Thermal/Thin Films/Doping
Ongoing Activities

- Verify L_g scaling for 2009 publication
- New modeling effort with PIDS in 2009
- Re-examine timing of innovation insertions and bulk CMOS end-of-life
- Contact resistance calculations – definitions, models, agreement between FEP, PIDS, and Interconnect

Etch
2008 Highlights

- New ORTC MPU/ASIC L_g scaling incorporated
- Gate CD control color changed to white through 2011 and to yellow for 2012 reflecting the new L_g scaling

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
MPU Physical Gate Length (nm)	32	29	27	24	22	20	18	17	15
L_{gate} 3 σ variation (nm) [Z]	3.82	3.49	3.18	2.9	2.65	2.42	2.21	2.02	1.84
Total maximum allowable lithography 3 σ (nm) [AA]	3.31	3.02	2.76	2.52	2.3	2.1	1.91	1.75	1.59
Total maximum allowable etch 3 σ (nm), including photoresist trim and gate etch [AA]	1.91	1.74	1.59	1.45	1.33	1.21	1.1	1	0.92
Resist trim maximum allowable 3 σ (nm) [AB]	1.1	1	0.92	0.84	0.77	0.7	0.64	0.58	0.53
Gate etch maximum allowable 3 σ (nm) [AB]	1.56	1.42	1.3	1.19	1.08	0.99	0.9	0.82	0.75

Etch
Ongoing Activities

- Verify L_g scaling trend in 2009
- Adjust tables in 2009, as necessary
- Re-examine physical gate length variation allowance sharing between litho/trim/etch

Stacked DRAM
2008 Highlights

- **Incorporate new ORTC DRAM scaling for 2007-2009**

Table FEP5	*DRAM Stacked Capacitor Technology Requirements—Near and Long-term Years*								
Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) [A]	68	59	52	*45*	*40*	*36*	*32*	*28*	*25*
Cell size factor a [B]	6	6	6	6	6	6	6	6	6
Cell size (μm^2) [C]	0.028 =0.14x0.204	0.021 =0.12x0.177	0.016 =0.10x0.156	0.012 =0.090x0.14	0.0096 =0.080x0.12	0.0077 =0.071x0.11	0.0061 =0.064x0.96	0.0048 =0.057x0.085	0.0048 =0.051x0.076
Storage node size (μm^2) [D]	0.00925 =0.068x0.14	0.00696 =0.053x0.12	0.0054 =0.052x0.10	0.0041 =0.045x0.090	0.0032 =0.040x0.080	0.0026 =0.036x0.071	0.002 =0.032x0.064	0.0016 =0.032x0.064	0.0013 =0.025x0.051

Trench DRAM
2008 Highlights

- **Trench DRAM no longer being scaled past 58nm technology generation**
- **Entries from 2009 to 2022 deleted**
- **Table to be removed from 2009 publication**

Table FEP6	*DRAM Trench Capacitor Technology Requirements—Near and Long-term Years*								
Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ pitch "F" (nm)	65	57	~~60~~	~~45~~	~~40~~	~~36~~	~~32~~	~~28~~	~~25~~
Cell size factor "a" [A]	8	8	~~8~~	~~8~~	~~8~~	~~8~~	~~8~~	~~8~~	~~8~~
Cell size (μm^2) [B]	0.045	0.028	~~0.018~~	~~0.016~~	~~0.0128~~	~~0.0104~~	~~0.0082~~	~~0.0063~~	~~0.005~~
Trench structure	bottled	bottled	~~bottled~~	~~bottled~~	~~bottled~~	~~bottled~~	~~bottled~~	~~bottled~~	~~bottled~~
Trench bottle circumference (nm) [C]	549	483	~~399~~	~~374~~	~~333~~	~~300~~	~~266~~	~~233~~	~~208~~
Trench etch depth (μm) [D]	6.8	6	~~6.8~~	~~6.6~~	~~6~~	~~4.6~~	~~4~~	~~3.7~~	~~3.4~~
Bottled trench depth (μm) [E]	6	5.3	~~5.4~~	~~4.8~~	~~4.3~~	~~3.8~~	~~3.3~~	~~3.4~~	~~2.8~~
Storage node size (μm^2) [F]	3.3	2.6	~~2~~	~~1.8~~	~~1.4~~	~~1.1~~	~~0.9~~	~~0.7~~	~~0.6~~
Trench surface area enhancement factor (HSG) [G]	1.2	1	~~1~~	~~1~~	~~1~~	~~1~~	~~1~~	~~1~~	~~1~~
Cell capacitance (fF) [H]	35	30	~~25~~	~~25~~	~~25~~	~~25~~	~~25~~	~~25~~	~~25~~
teq at Cs (nm) [I]	3.9	3.5	~~2.8~~	~~2.5~~	~~2~~	~~1.6~~	~~1.2~~	~~1~~	~~0.8~~
Trench top opening (nm) [J]	98	81	~~70~~	~~63~~	~~56~~	~~50~~	~~45~~	~~39~~	~~35~~
Trench etch aspect ratio [K]	70	74	~~83~~	~~89~~	~~89~~	~~89~~	~~89~~	~~94~~	~~97~~
Capacitor structure	Cup SIS	Cup MIS	~~Cup~~ ~~MIS~~	~~Cup~~ ~~MIM~~	~~Cup~~ ~~MIM~~	~~Cup~~ ~~MIM~~	~~Cup~~ ~~MIM~~	~~Cup~~ ~~MIM~~	~~Cup~~ ~~MIM~~

DRAM
Ongoing Activities

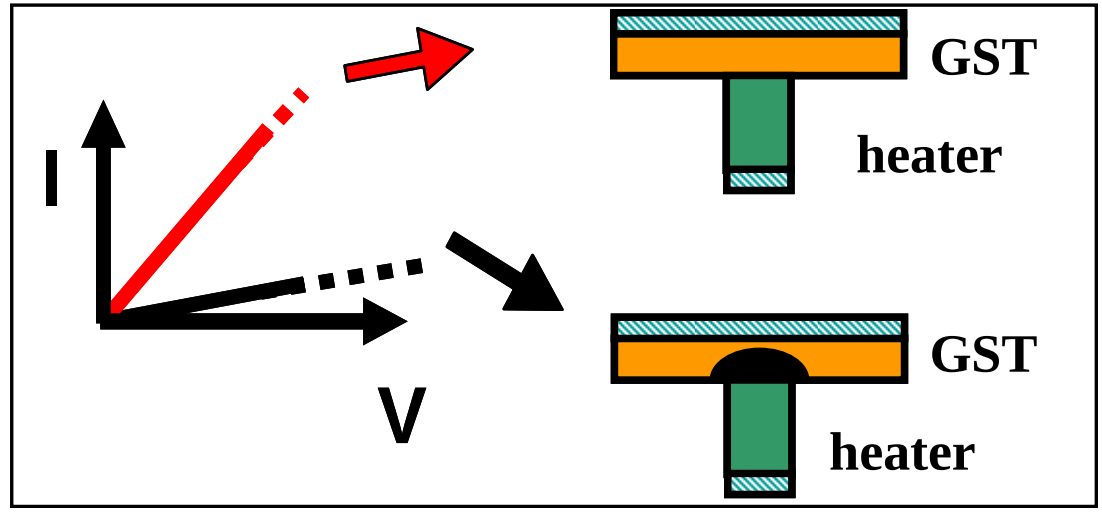
- For 2009 consider adding scaling parameters related to the transistors in the array and periphery

Flash
2008 Highlights

- no major changes
- Potential solutions updates for STI filling
- push out implementation of high-k materials to 32nm generation or beyond
- General update of color coding
- potential solutions for engineered barrier tunnel dielectrics

PCRAM
2008 Highlights

- heater material requirements updated resistivity variation scaling – 5% vs 1% - related to dimensional scaling and current density



Flash / PCM
Ongoing Activities

- review end of Floating Gate Flash
- consider adding table for Charge Trapping Flash parameters in 2009
- consider adding parameters to PCRAM tables, such as interconnect dielectrics

FeRAM
2008 Highlights

- **Correct inconsistencies in FeRAM roadmap table between PIDS and FEP.**
  - **Technology node, F (nm)**

	2007	2010	2013	2016	2019
PIDS	180	130	90	90	65
FEP	180	150	130	90	65

  - **Capacitor footprint at 2016 (capacitor size 0.041 um^2)**

PIDS	Red
FEP	Yellow

  - **Proposal to PIDS NVM table owner to adopt FEP values & color for 2008 update.**
- **Correct stated scaling factor to .85x/3yr on page 55**
- **Add missing Potential Solutions Figure**