INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2006 UPDATE

FRONT END PROCESSES

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FRONT END PROCESSES

SUMMARY

Updates to the Front End Processes (FEP) chapter in 2006 have been minimal except in the area of thermal/thin films (see below). A few changes have been made to the FEP Difficult Challenges, Table 66a and Table 66b. In Table 66a we recognize that local strain has been integrated into current IC manufacturing and should be extendable to at least the 32 nm generation. In Table 66b we note that continued scaling of local strain will be a challenge beyond the 32 nm generation. We also note that implementation of high-κ gate stack materials in low standby power (LSTP) applications should be achievable, while implementation of these materials in high performance (HP) logic and low operating power (LOP) applications is still considered a difficult challenge. Introduction of 450 mm wafers in 2012 is still considered a difficult challenge facing numerous issues.

In the Starting Materials and Surface Preparation sections of this chapter we included a few minor updates in the color indications. Starting Materials particle metrics for 2011 have been changed from yellow to white and Surface Preparation material loss metrics for 2008 and beyond have been changed from red to "interim solutions are known". In the Surface Preparation Potential Solutions chart, Figure 57, we have indicated a delay in the potential introduction of supercritical CO_2 methods to manufacturing.

Updates for Thermal/Thin Films, Doping and Etching are centered on the timing for introduction of high-κ/metal advance gate stack materials and also for introduction of fully depleted silicon on insulator (FDSOI). The updates to Table 69a reflect a push back of the introduction of advanced gate materials for HP logic and for LOP to the year 2010. The introduction of advanced gate stack materials for LSTP remains in 2008. Also, the introduction of FDSOI for HP logic has been pushed back to 2010. These changes for advanced gate stack and FDSOI were made after extensive discussion with the Process Integration, Devices, and Structures (PIDS) Technology Working Group (TWG) and reflect the expected readiness of these new materials for commercial production.

For dynamic random access memory (DRAM) Stacked Capacitor we have made some changes in the potential solutions chart, Figure 61, for high-κ materials. For DRAM Trench Capacitor the use of NO dielectric has been extended through the 70 nm generation, with high-κ materials being introduced at the 65 nm generation. In addition, for the DRAM Trench Capacitor new integration schemes to be introduced at 40 nm will reduce the thermal budget for the cell capacitor. Thus a more aggressive scaling of the capacitance equivalent oxide thickness (CET) will be possible. As a consequence the trench aspect ratio can be kept at less than 100 down to the 28 nm generation.

For Flash Non-Volatile Memory a new row has been added to Table 72 for the "STI Filling Aspect Ratio". A footnote has also been added to Table 72 to explain this new row. For Phase Change Memory (PCM) a new table has been introduced to indicate two important metrics for PCM scaling: phase change material conformality and minimum operating temperature.

Finally, for ferroelectric RAM (FeRAM), a note has been added about the implementation issues with BFO ($BiFeO_3$) and other ferroelectric materials. In addition the FeRAM Potential Solutions chart, Figure 65, has been updated to include BFO.

DIFFICULT CHALLENGES

Table 66a Front End Processes Difficult Challenges—Near-term Years UPDATED

Difficult Challenges ≥ 32 nm	*Summary of Issues*
New gate stack processes and materials	Extension of oxynitride gate dielectric materials to < 1.0 nm EOT for high-performance MOSFETs, consistent with device reliability requirements
	Control of boron penetration from doped polysilicon gate electrodes while minimizing depletion of dual-doped polysilicon electrodes
	Introduction and process integration of high-κ gate dielectrics ~~stack materials~~ and processes for high-performance, low operating ~~and low standby~~ power MOSFETs
	~~CMOS integration of enhanced channel mobility in both NMOS and PMOS devices, using local and global strained layers~~
	Introduction of dual metal gate electrodes with appropriate work function
	Control of silicon loss at spacer etch and gate etch needs to be much tighter on thin SOI and SiGe wafers, where the total silicon thickness is 20–50 nm
	Removal of high-κ dielectric without loss of the underlying silicon, especially in the case of SOI or non planar devices
	Metrology issues associated with gate dielectric film thickness and gate stack electrical and materials characterization
	Control of gate etch processes that yield a physical gate length that is considerably smaller than the feature size printed in the resist, while maintaining <12% overall 3-sigma control of the combined lithography and etch processes
Critical dimension and effective channel length (L_{eff}) control	Control of profile shape, edge roughness, line and space width for isolated as well as closely-spaced fine line patterns
	Control of self-aligned doping processes and thermal activation budgets to achieve L_{eff} control
	Maintenance of CD and profile control throughout the transition to new gate stack materials and processes
	CD and etch metrology
	Site flatness to ensure effective lithographic printing
	Development and introduction of very high-κ DRAM capacitor dielectric layers
Introduction and CMOS integration of new memory materials and processes	Migration of DRAM capacitor structures from silicon-insulator-metal to metal-insulator-metal
	Integration and scaling of FeRAM ferroelectric materials
	Scaling of Flash interpoly and tunnel dielectric layers may require high-κ
	Limited temperature stability of high-κ and ferroelectric materials challenges
	CMOS Integration
	Contamination, composition, and structure control of channel/gate dielectric interface as well as gate dielectric/gate electrode interface
Surfaces and interfaces—structure, composition, and contamination control	Interface control for DRAM capacitor structures
	Maintenance of surface and interface integrity through full-flow CMOS processing
	Statistically significant characterization of surfaces having extremely low defect concentrations for starting materials and pre-gate clean surfaces
	Measurement of back surface particles at/near edge wafer edge (including bevel) has no solution
	Measurement and understanding of clustering of particles needs significant data to define future specification
	Little information associating back surface particles and the effect on yield
	Doping and activation processes to achieve shallow source/drain regions having parasitic resistance that is less than ~17–33% of ideal channel resistance ($=V_{dd}/I_{on}$)
Scaled MOSFET dopant introduction and control	Control of parasitic capacitance to achieve less than ~23–29% of gate capacitance, consistent with acceptable Ion and minimum short channel effect
	Achievement of activated dopant concentration greater than solid solubility in dual-doped polysilicon gate electrodes
	Formation of continuous self-aligned silicide contacts over shallow source and drain regions. Formation of elevated junctions and silicides on FDSOI wafers
	Metrology issues associated with 2D dopant profiling

Table 66b Front End Processes Difficult Challenges—Long-term Years UPDATED

Difficult Challenges < 32 nm	*Summary of Issues*
Continued scaling of planar CMOS devices	Continued application of strain engineering techniques
	Higher κ gate dielectric materials including temperature constraints
	Metal gate electrodes with appropriate work function
	Sheet resistance of clad junctions
	CD and L_{eff} control
	Chemical, electrical, and structural characterization
Introduction and CMOS integration of non-standard, double gate MOSFET devices	Devices are needed starting from 2011 and may be needed as early as 2007 (this is a backup for high-κ materials and metal gates on standard CMOS)
	Selection and characterization of optimum device types
	CMOS integration with other devices, including planar MOSFETs
	Introduction, characterization, and production hardening of new FEP unit processes
	Device and FEP process metrology
	Increased funding of long term research
	Introduction of strained silicon in the structural configuration for advanced non-classical CMOS
Starting silicon material alternatives greater than 300 mm diameter require the start of wafer manufacturing development in year 2005	Need for future productivity enhancement dictates the requirement for a next generation, large silicon substrate material
	Historical trends suggest that the new starting material have nominally twice the area of present generation substrates, e.g., 450 mm
	Economies of the incumbent Czochralski crystal pulling, wafer slicing, and polishing processes are questionable beyond 300 mm; research is required for a cost-effective substrate alternative to bulk silicon
	If 450 mm wafers are to become available for production in 2012 as currently forecasted, wafer manufacturing is already behind schedule and must be implemented in 2005–2006
	Enhanced coordination is required amongst Starting Materials, Factory Integration, Yield Enhancement and the IRC to more effectively assess the anticipated onset of 450 mm use
New memory storage cells, storage devices, and memory architectures	Scaling of DRAM storage capacitor beyond $6F^2$
	Further scaling of Flash memory interpoly and tunnel oxide thickness
	FeRAM storage cell scaling
	Introduction of new memory types and storage concepts (Candidates—MRAM, phase-change memory for 2010, and single electron, molecular, nano-floating products beyond 2010)
Surface and interface structural, contamination, and compositional control	Achievement and maintenance of structural, chemical, and contamination control of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface
	Metrology and characterization of surfaces that may be horizontally or vertically oriented relative to the chip surface
	Achievement of statistically significant characterization of surfaces and interfaces that may be horizontally or vertically oriented relative to the chip surface

TECHNOLOGY REQUIREMENTS AND POTENTIAL SOLUTIONS

STARTING MATERIALS

Table 67a Starting Materials Technology Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	DRAM Total Chip Area (mm^2)	88	139	110	74	117	93	74	117	93
	DRAM Active Transistor Area (mm^2)	23.1	36.2	29.5	23.1	36.4	29.1	23.1	36.0	29.1
	MPU High-Performance Total Chip Area (mm^2)	246	195	310	246	195	310	246	195	310
	MPU High-Performance Active Transistor Area (mm2)	25.1	20.0	31.7	25.1	20.0	31.7	25.1	20.0	31.7
	General Characteristics * (99% Chip Yield) [A, B, C]									
	Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)**	300	300	300	300	300	300	300	450	450
	Edge exclusion (mm)	2	2	1.5	1.5	1.5	1.5	1.5	1.5	1.5
WAS	Front surface particle size (nm), latex sphere equivalent [D] [E]	≥90	≥90	≥90	≥90	≥65	≥65	≥65	≥45	≥45
IS	Front surface particle size (nm), latex sphere equivalent [D] [E]	≥90	≥90	≥90	≥90	≥65	≥65	≥65	≥45	≥45
WAS	Particles (cm^{-2})	≤0.35	≤0.17	≤0.18	≤0.17	≤0.16	≤0.17	≤0.17	≤0.17	≤0.17
IS	Particles (cm^{-2})	≤0.35	≤0.17	≤0.18	≤0.17	≤0.16	≤0.17	≤0.17	≤0.17	≤0.17
WAS	Particles (#/wafer)	≤238	≤116	≤123	≤120	≤113	≤115	≤115	≤265	≤271
IS	Particles (#/wafer)	≤238	≤116	≤123	≤120	≤113	≤115	≤115	≤265	≤271
	Site flatness (nm), SFQR 26 mm × 8 mm site size [F, R]	≤80	≤70	≤65	≤57	≤50	≤45	≤40	≤35	≤32
	Nanotopography, p-v, 2 mm diameter analysis area [Q]	≤20	≤18	≤16	≤14	≤13	≤11	≤10	≤9	≤8
	Polished Wafer * (99% Chip Yield)									
	The LLS requirement is specified for particles only; discrimination between particles and COPs is required (see General Characteristics) [D, E]									
	Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) [G]	≤1.39	≤1.15	≤1.03	≤0.85	≤0.71	≤0.81	≤0.52	≤0.43	≤0.37
	Oxidation stacking faults (OSF) (MPU) (cm^{-2}) [G]	≤0.37	≤0.32	≤0.27	≤0.23	≤0.19	≤0.16	≤0.14	≤0.12	≤0.10
	Epitaxial Wafer * (99% Chip Yield)									
	Total Allowable Front Surface Defect Density is The Sum of Epitaxial Large Structural Defects, Small Structural Defects and Particles (see General Characteristics) [H, I]									
	Large structural epi defects (DRAM) (cm^{-2}) [J]	≤0.011	≤0.007	≤0.009	≤0.014	≤0.009	≤0.011	≤0.014	≤0.009	≤0.011
	Large structural epi defects (MPU) (cm^{-2}) [J]	≤0.004	≤0.005	≤0.003	≤0.004	≤0.005	≤0.003	≤0.004	≤0.005	≤0.003
	Small structural epi defects (DRAM) (cm^{-2}) [K]	≤0.023	≤0.014	≤0.018	≤0.027	≤0.017	≤0.022	≤0.027	≤0.017	≤0.022
	Small structural epi defects (MPU) (cm^{-2}) [K]	≤0.008	≤0.010	≤0.006	≤0.008	≤0.010	≤0.006	≤0.008	≤0.010	≤0.006
	Silicon-On-Insulator Wafer* (99% Chip Yield)[R]									
	Edge exclusion (mm) ***	2	2	1.5	1.5	1.5	1.5	1.5	1.5	1.5
	Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (nm) [L]	58–100	53–91	48–83	44–76	40–70	37–65	34–60	31–45	29–42
	Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3s) (nm) [M]	20–36	19–34	18–33	16–30	15–29	15–28	14–27	13–15	13–15
	Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3s) (nm) [N]	48–80	42–70	38–64	34–56	30–50	26–44	24–40	22–36	18–32
	D_{LASOI}, Large area SOI wafer defects (DRAM) (cm^{-2}) [O]	≤0.011	≤0.007	≤0.009	≤0.014	≤0.009	≤0.011	≤0.014	≤0.014	≤0.012

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
D_{LASOI}, Large area SOI wafer defects (MPU) (cm^{-2}) [O]	≤0.004	≤0.005	≤0.003	≤0.004	≤0.005	≤0.003	≤0.004	≤0.004	≤0.003
D_{SASOI}, Small area SOI wafer defects (DRAM) (cm^{-2}) [P]	≤0.218	≤0.139	≤0.170	≤0.218	≤0.138	≤0.173	≤0.218	≤0.139	≤0.173

** Parameters define limit values, independent predictors of yield, mathematically or empirically modeled at 99%. limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one limit value "at a time"; other parameter values are most likely near median value, thereby insuring total yield for all parameters is at least 99%.*

*** Values expressed in a per wafer format are calculated assuming the maximum stated wafer diameter, although that diameter likely may not be the predominant one for the corresponding technology generation. Although 450 mm is colored yellow indicating manufacturable solutions are know, it could have easily been colored red, because there has been no acceptable economic solution for funding identified by the industry.*

**** Edge exclusion is repeated in the Silicon on Insulator Wafer section because of inherent limitations associated with certain SOI wafer production techniques that differ from polished and epitaxial wafer edge exclusion capabilities.*

Meaning and Color Coding of Left Box	***Meaning and Color Coding of Right Box***
Technology Requirements Value and Supplier Manufacturing Capability by Color	**Metrology Readiness Capability by Color**
Manufacturable solutions exist, and are being optimized	*Manufacturable solutions exist, and are being optimized*
Manufacturable solutions are known	*Manufacturable solutions are known*
Manufacturable solutions are NOT known	***Manufacturable solutions are NOT known***

Notes for Table 67a and b

[A] Surface metals are empirically grouped into three classes[1, 2]: (a) Mobile metals that may be easily cleaned such as Na and K and may be modeled by taking the flat-band shift of a capacitance-voltage (CV) test approximately 50 mV for a representative 1 nm EOT; (b) metals that dissolve in silicon or form silicides such as Fe, Ni, Cu, Cr, Co, Al, Zn; and (c) major gate-oxide-integrity (GOI) killers such as Ca. Each of these metals is taken at a maximum value of $1 \times 10^{10}/cm^2$ for all subsequent technology generations. The surface concentration of carbon atoms after cleaning is based on the assumption that a 10% (7.3×10^{13} atoms/cm^2) carbon atom coverage on a bare silicon (100) surface can be tolerated during device fabrication. Organics/polymers are therefore modeled approximately 0.1 of a monolayer, $\leq 1 \times 10^{14}$C atoms/cm^2. Surface organic levels are highly dependent on wafer packaging, on hydrophobic or hydrophilic wafer surface conditions, and on wafer storage conditions such as temperature, time and ambient.

Total bulk Fe consistent with recombination lifetime, τ_r, as measured by the SPV technique (for lightly doped p-type material) at low injection level is held at $1 \times 10^{10}/cm^3$ for all subsequent technology generations.[3] Note that the bulk Fe concentration (at/cm_3) cannot be converted to surface concentration (at/cm^2) via wafer thickness. Recombination lifetime $\tau_r = (L^2)/D_n$, where L = minority-carrier diffusion length and D_n = minority-carrier diffusion coefficient at 27°C.[4] The diffusion length is taken equal to the wafer thickness, resulting in a τ_r value of 350 μsec. The allowable lifetime is doubled to ensure a sufficient safety factor, resulting in a final value of 700 μsec. Appropriate technique(s) to control, stabilize and passivate surface effects is required, depending on the technique (SPV, PCD, etc.), especially for a bulk lifetime greater than 20 μsec. For any technique other than SPV, the injection level must be noted. No oxygen precipitation in sample, no back-side mechanical damage, and resistivity of 5–20 Ohm-cm recommended.

[B] Instrumentation choice, target values, and spatial frequency range (scan size) for front-surface microroughness are selected based on application. Power spectral density analysis is recommended to utilize full accessible range of instruments. A typical value for polished wafers is ≤ 0.1 nm (RMS) for all CD generations. Epitaxial, annealed and SOI wafers have values that are typically higher than polished wafers while still meeting the user's requirement.

[C] The oxygen concentration may be specified depending on the particulars of the IC user based on IC process requirements and is generally in the range of 18–31 ppma (SEMI M44-0702, refer to ASTM F121-79).[5] With advanced crystal growth technologies, bulk micro defects (BMDs) can be achieved independent of the interstitial oxygen concentration. The importance of BMDs for gettering has recently again been emphasized and may be especially important in those IC fabrication cases with low thermal budgets.[6] Co-doping techniques (such as nitrogen and carbon) can be used to enhance oxygen precipitation so may be particularly well suited for low thermal budget device processes. Additionally, certain growth methods coupled with heat treatments can also enhance the precipitation of oxygen. Not all device processes, however, require the presence of BMDs. BMDs for internally gettered polished wafers may be generically taken as greater than approximately $1 \times 10^8/cm^3$ after IC processing. BMD density is measured using ASTM F-1239.

[D] Critical front surface particle size = K_1F, [K_1=1] where F is the DRAM half-pitch and is used to calculate required particle densities at the given technology generation. Particle sizes reported in Tables 67a and b are held constant for several generations before being reduced, due to metrology capability. Particle densities are extracted from the conventional Maly Yield Equation[7] {$Y = \exp[-(D_P R_P) A_{eff}]$, where A_{eff}, is the effective chip area $A_{eff} = 2.5*F^2T + (1-aF^2T/A_{chip})A_{chip}*0.18$, "a" is the DRAM cell fill factor (see Table 70a) and T = number of transistors or bits/chip per technology generation}$*(K_1F/PS)^2$, where PS is the particle size reported in the table for the respective technology generation. This method therefore applies the square law to calculate the predicted densities for the respective reported particle sizes, using the density for the critical front surface particle size obtained from the Maly Yield Equation as the reference density at each respective technology generation. The kill factor R_P is assumed to be 0.2, although the kill factor may be very dependent upon the specifics of the DRAM fab. The relationship between actual defect size and associated LSE (latex sphere equivalent) size depends on defect type and scanner geometry. The current particle size threshold capability for SOI wafers is approximately 100 nm, due to the altered response in the optical metrology tools, compared to polished or epitaxial wafers.

[E] Detailed back-surface particle information is not included in Table 67, since, in practice, lithography concerns are being met by identifying these defects visually. This perhaps suggests that only large defects are of impact. If desired, the calculations may be made using the following model for back-surface particle size and density. The front-surface height elevation, H, due to a back-surface particle of size, D, under a back-surface film of thickness, T, and a wafer thickness, W, may be expressed as [(xD +xT +W) – (T + W)], which may be reduced to [(xD) – (1-x)T], where x = 0.6 is the compression of the particle and back-surface film due to the pressure of the chuck on the wafer. Assuming a front-surface elevation of 2(CD) results in a 100% lithographic printing failure, the back-surface particle size is expressed as: D = [(2/0.6) (F) + (0.4/0.6) (T)], where F and T are expressed in nm. In this model, T may be set equal to 100 nm, for example. Back-surface particles modeled for 99% yield: $Y = \exp(-D_P R_P A_{eff})$ [7]. $R_P = 1.0$, $A_{eff} = A_{chip} \times 0.03 \times 0.8$, where 0.03 corresponds to 3% of the chip area touching the chuck and 0.8 corresponds to 80% of the effective chip area that is degraded by effects of the back-surface particle on the front-surface de-focus effect. D_p, then, represents the density of defects allowable in visible inspection for backside particles. The equation for the "killer" backside particle diameter strongly depends on two assumptions that are process dependent. The first is that a focal plane excursion of 2 CD is required for a 100% assured printing failure. Although a process window this wide may exist in many cases, some tightly specified exposures maybe less tolerant to focal plane deviations. This would lead to a smaller particle becoming a backside killer. The second assumption is that the particles and film are both compressed to 60% of their original dimension. This assumption might not be true if the particle were made of a material much harder than the film or the particle was similar in hardness to silicon and there was no backside film (T=0). Either of these circumstances allows a smaller particle to become a possible backside killer. The backside yield equation assumes that the entire chip is killed by a back-surface particle generating a front-surface focal plane deviation during lithography (the critical particle diameter is that value accordingly used in the equation, or larger). This occurs because a particle with diameter much smaller than the thickness of the wafer may create a bulge on the front surface up to 10 mm in diameter, so a significant portion of the field is out of focus, and the chip does not yield. A mitigating circumstance occurs if the particle is near the die edge, however, since the bulge at the die edge will tend to create only an apparent local tilt in the field that can be accommodated by a scanning stepper leveling system. This gives rise to the 80% effective degraded area.

[F] The metric for site flatness should be matched to the type of exposure equipment used in leading edge applications, which implies scanning steppers for critical levels. While SFSR may be the most appropriate metric, it has failed to gain appreciable support in the industry. Historical reference to SFQR remains strong and it appears inevitable that this metric will continue to be used in the future. To more closely emulate practical experience of the scanning stepper, the effective site size for local site flatness is being modified to 26 mm × 8 mm accordingly. Full-field steppers with square fields (nominally 22 × 22 mm) may still be utilized for non-critical levels although these are increasingly being phased out. In either case, the metric value is approximately equal to F for dense lines (DRAM half pitch). Partial sites should be included. Also note that flatness metrology requires sufficient spatial resolution to capture topographical features relevant for each technology generation.

[G] OSF density empirically modeled by $K_3 (F)^{1.42}$; F in nm; $K_3 = 2.75 \times 10^{-3}$. [8] The utilization of the OSF density relation by extension into technology generation regimes, not envisioned in the original experimental analysis, will require re-assessment. Test at 1100°C, 1 hour wet oxidation, strip oxide/etch;OSF is more difficult to control in n-type material.

[H] Other epitaxial defects such as hillocks and mounds should also be accounted for, but an appropriate yield model is not available. Accurate segregation based upon defect morphology is also not generally available with today's metrology.

[I] Desired epitaxial layer thickness tolerance is ± 4% for a 2 to 10 mm center-point epitaxial layer thickness target value but may be affected on p/p^+ structures due to lack of autodoping suppression via backside film deposition, resulting from incompatibility with 300 mm wafers. In the case of p/p^- epi, the minimum epi layer thickness is designed to avoid the possible influence of bulk grown-in defects such as COPs; this consideration is less critical for p/p^+ where the COPs are significantly reduced in the p^+ substrate compared to p^-.

[J] Large structural epi defects (large area defects >1 μm LSE signal) modeled at 99% yield where $Y = \exp(-D_{LAD} R_{LAD} A_{chip})$,[6] where $R_{LAD} = 1$ and A_{chip} applies to DRAM and high-performance MPU as appropriate. METROLOGY NOTE: Many current generation scanning surface inspection systems (SSIS) cannot reliably size surface features with LSE signals greater than about 0.5μm due to the light scattering characteristics of these large structural epi defects and the optical design of the tool. Further, a metrology gap clearly exists since production worthy tools are not available that can separate large structural epi defects from other features like large particles as well as identify and count epitaxial stacking faults.

[K] Small structural epi defects (≤ 1μm LSE signal) modeled at 99% yield where $Y = \exp(-D_{SF} R_{SF} A_{chip})^6$ where $R_{SF} = 0.5$ and A_{chip} applies to DRAM and high-performance MPU as appropriate. Starting Materials uses the DRAM at production and the MPU high-performance MPU areas. METROLOGY NOTE: A metrology gap clearly exists since production worthy tools are not available that can identify and count small structural epi defects.

[L] The silicon final device layer thickness (partially depleted) is obtained by 2 × MPU physical gate length (with a range in nominal values of ± 25%). Range of target value refers to the center point measurement with uniformity to indicate within-wafer maximum positive or negative % deviation from the center value. The final device silicon is less than incoming material due to Si consumption during device fabrication. In the table, the starting material layer thickness is shown. For years 2003 to 2009 it is obtained by adding 10 nm to the lower value in the range and 20 nm to the higher value in the range. After 2009, 10 nm is added to both values in the range in order to translate the device thickness into the starting material thickness. Si loss depends on processing conditions used—it is assumed here that processing parameters are controlled more tightly after 2009. It should be noted that partially depleted silicon on insulator solutions are shown for all years but may generally not be compatible with more aggressively scaled technology generations.

[M] The silicon final device thickness (fully depleted) is obtained by 0.4 × MPU physical gate length prior to 2008, 0.35 x MPU physical gate length 2008 to 2011, 0.3 x MPU physical gate length at 2012 and thereafter (with a range in nominal values of ± 25%). Range of target value refers to the center point measurement with uniformity to indicate within-wafer maximum positive or negative % deviation from the center value. The final device silicon is less than incoming material due to consumption during device fabrication. In the table the starting material layer thickness is shown. For years 2003 to 2009 it is obtained by adding 10 nm to the lower value in the range and 20 nm to the higher value in the range. After 2009, 10 nm is added to both values in the range in order to translate the device thickness into the starting material thickness. Si loss depends on processing conditions used—it is assumed here that processing parameters are controlled more tightly after 2009.

[N] The BOX thickness for fully depleted devices is taken as the 2 × MPU physical gate length. BOX scales with gate length to help to control short channel effects and heat dissipation. Range in nominal target value of ± 25% allows for trade-off between the BOX and silicon thickness to control short channel effects in the fully depleted SOI devices. NOTE: For partially depleted SOI devices, the BOX thickness has less of a direct impact on device parameters. Considerations of BOX capacitance, circuit heat dissipation, gettering, BOX electrical integrity, SOI wafer manufacturing capabilities, wafer quality and wafer cost have driven the choice of the BOX thickness values. The BOX thickness is expected to remain between 100–200 nm for the timeframe of partially depleted SOI devices.

[O] Large area SOI (LASOI) wafer defects with yield of 99%; $Y = \exp(-D_{LASOI} R_{LASOI} A_{chip})$,[6] D_{LASOI} = LASOI defect density, R_{LASOI} =1.0 (best present estimate).

[P] Small area SOI (SASOI) wafer defects with yield of 99%; $Y = \exp(-D_{SASOI} R_{SASOI} A_{eff})$, [6] *$D_{SASOI}$ = SASOI defect density, R_{SASOI} = 0.2 (best present estimate). Sources of SASOI can include COPs, metal silicides, or local SiO_2 islands in the top silicon layer. These SASOI defects may also be detected by localized light scattering (LLS) measurements.* [9, 10, 11]

[Q] Peak-to-valley threshold, 2 mm diameter analysis area. Maximum p-v reading taken as CD/4, based on extrapolation of wafer supplier process capability for 180–90 nm technology generations, plus published data on linewidth distortion for sub-100 nm critical dimensions.

[R] The magnitude of within-wafer variation of various wafer parameters changes over different length scales, depending on the nature of the mechanisms that produce them. The impact on subsequent device manufacturing caused by these variations, which occur at different spatial wavelengths, also depends on the nature of the fab processes and resulting devices. For instance, parameters governed by gas flow and temperature gradient variations, such as CVD layer thickness, typically vary appreciably only over fairly long distances, of the order of millimeters to centimeters. It is often adequate to measure such slowly varying parameters at only a modest number of locations on the wafer, using a metrology tool with a fairly low spatial resolution, in order to control such processes. Other parameters, such as wafer surface topography, vary on multiple length scales with different impacts in the fab. At very large length scale (tens of centimeters), wafer surface height variations are many microns in magnitude (e.g. bow and warp), and can affect various mechanical properties of the wafer. At length scales on the order of one centimeter, the surface variations are fractions of a micron in height. These variations (i.e. site flatness) generally are not critical to mechanical shape of the wafer, but are vital to depth of focus in lithography. At still smaller length scales of a few millimeters or less, the surface height variations are on the order of tens of nanometers high. They do not cause focus failures in lithography, but can produce line width variations in gate lengths and polishing removal uniformity problems in CMP. On the length scale of microns, surface roughness variations are of the order of Angstroms, but can cause gate oxide integrity problems. As another example, in fully depleted SOI wafers, thickness variations of the top silicon layer can cause transistor threshold voltage variation die-to-die (at centimeter length scale), within-die (at millimeter length scale), and conceivably, even transistor-to-transistor (on a sub-micron scale). To control parameter variations across a large range of spatial wavelengths requires a tool capable of measuring the whole wafer to capture long wavelength components, but with a very high density of data points (with correspondingly small sampled area) to capture small wavelength components. The spatial wavelength requirements thus have a profound effect on metrology capability. Methods that work well at long spatial wavelengths may become unsuitable at small spatial wavelengths due to measurement throughput limitations and/or inadequate spatial resolution. Metrology grades in this table reflect current spatial wavelength requirements. Future process and device developments that demand measurement at shorter spatial wavelengths may alter these capability grades in unforeseen ways.

Table 67b Starting Materials Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*D ½*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	M
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*M*
DRAM Total Chip Area (mm^2)	**74**	**117**	**93**	**74**	**117**	**93**	**74**	D ½
DRAM Active Transistor Area (mm^2)	**23.1**	**36.7**	**28.6**	**23.1**	**36.7**	**29.1**	**19.6**	D ½
MPU High-Performance Total Chip Area (mm^2)	**246**	**195**	**310**	**246**	**195**	**310**	**246**	M
MPU High-Performance Active Transistor Area (mm2)	**25.1**	**20.0**	**31.7**	**25.1**	**20.0**	**31.7**	**25.1**	M
*General Characteristics * (99% Chip Yield) [A, B, C]*								
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)**	**450**	**450**	**450**	**450**	**450**	**450**	**450**	*D ½, M*
Edge exclusion (mm)	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	*D ½, M*
Front surface particle size (nm), latex sphere equivalent [D][E]	**≥45**	**≥32**	**≥32**	**≥32**	**≥22**	**≥22**	**≥22**	*D ½, M*
Particles (cm^{-2})	**≤0.17**	**≤0.17**	**≤0.17**	**≤0.17**	**≤0.18**	**≤0.18**	**≤0.21**	*D ½*
Particles (#/wafer)	**≤271**	**≤268**	**≤261**	**≤268**	**≤283**	**≤283**	**≤233**	*D ½*
Site flatness (nm), SFQR 26 mm × 8 mm site size [F, R]	**≤28**	**≤25**	**≤22**	**≤20**	**≤18**	**≤16**	**≤14**	*D ½, M*
Nanotopography, p-v, 2 mm diameter analysis area [Q]	**≤7**	**≤6**	**≤6**	**≤5**	**≤4**	**≤4**	**≤4**	*M*
*Polished Wafer * (99% Chip Yield)*								
The LLS requirement is specified for particles only; discrimination between particles and COPs is required (see General Characteristics) [D, E]								
Oxidation stacking faults (OSF) (DRAM) (cm^{-2}) [G]	**≤0.32**	**≤0.27**	**≤0.22**	**≤0.19**	**≤0.16**	**≤0.14**	**≤0.12**	*D ½*
Oxidation stacking faults (OSF) (MPU) (cm^{-2}) [G]	**≤0.09**	**≤0.07**	**≤0.06**	**≤0.05**	**≤0.04**	**≤0.04**	**≤0.03**	*M*
*Epitaxial Wafer * (99% Chip Yield)*								
Total allowable front surface defect density is the sum of epitaxial large structural defects, small structural defects and particles (see General Characteristics) [H, I]								
Large structural epi defects (DRAM) (cm^{-2}) [J]	**≤0.014**	**≤0.009**	**≤0.011**	**≤0.014**	**≤0.009**	**≤0.011**	**≤0.014**	*D ½*
Large structural epi defects (MPU) (cm^{-2}) [J]	**≤0.004**	**≤0.005**	**≤0.003**	**≤0.004**	**≤0.005**	**≤0.003**	**≤0.004**	*M*
Small structural epi defects (DRAM) (cm^{-2}) [K]	**≤0.027**	**≤0.017**	**≤0.022**	**≤0.027**	**≤0.017**	**≤0.022**	**≤0.027**	*D ½*
Small structural epi defects (MPU) (cm^{-2}) [K]	**≤0.008**	**≤0.010**	**≤0.006**	**≤0.008**	**≤0.010**	**≤0.006**	**≤0.008**	*M*
Silicon-On-Insulator Wafer (99% Chip Yield)[R]*								
Edge exclusion (mm) ***	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	*M*
Starting silicon layer thickness (Partially Depleted) (tolerance ± 5%, 3σ) (nm) [L]	**27–38**	**25–35**	**23–32**	**22–30**	**21–28**	**19–26**	**18–24**	*M*
Starting silicon layer thickness (Fully Depleted) (tolerance ± 5%, 3s) (nm) [M]	**13–14**	**12–14**	**12–13**	**12–13**	**12–13**	**11–12**	**11–12**	*M*
Buried oxide (BOX) thickness (Fully Depleted) (tolerance ± 5%, 3s) (nm) [N]	**16–28**	**16–26**	**14–22**	**12–20**	**10–18**	**10–16**	**8–14**	*M*
D_{LASOI}, Large area SOI wafer defects (DRAM) (cm^{-2}) [O]	**≤0.014**	**≤0.012**	**≤0.011**	**≤0.007**	**≤0.009**	**≤0.009**	**≤0.009**	*D ½*
D_{LASOI}, Large area SOI wafer defects (MPU) (cm^{-2}) [O]	**≤0.004**	**≤0.003**	**≤0.003**	**≤0.003**	**≤0.005**	**≤0.005**	**≤0.005**	*M*
D_{SASOI}, Small area SOI wafer defects (DRAM) (cm^{-2}) [P]	**≤0.218**	**≤0.137**	**≤0.176**	**≤0.218**	**≤0.137**	**≤0.173**	**≤0.256**	*D ½*
D_{SASOI}, Small area SOI wafer defects (MPU) (cm^{-2}) [P]	**≤0.200**	**≤0.252**	**≤0.159**	**≤0.200**	**≤2.252**	**≤0,159**	**≤0.200**	*M*

**Parameters define limit values, independent predictors of yield, mathematically or empirically modeled at 99%. limit values rarely coincide for more than one parameter. A given wafer will generally not exhibit more than one limit value "at a time"; other parameter values are most likely near median value, thereby insuring total yield for all parameters is at least 99%.*

*** Values expressed in a per wafer format are calculated assuming the maximum stated wafer diameter, although that diameter likely may not be the predominant one for the corresponding technology generation. Although 450 mm is colored yellow indicating manufacturable solutions are know, it could have easily been colored red, because there has been no acceptable economic solution for funding identified by the industry.*
**** Edge exclusion is repeated in the Silicon on Insulator Wafer section because of inherent limitations associated with certain SOI wafer production techniques that differ from polished and epitaxial wafer edge exclusion capabilities.*

FRONT END SURFACE PREPARATION

Table 68a Surface Preparation Technology Requirements—Near-term Years UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*Driver*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*D ½*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*	*M*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*M*
	Wafer diameter (mm)	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**450**	**450**	*D ½, M*
	Wafer edge exclusion (mm)	**2**	**2**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	**1.5**	*D ½, M*
	Front surface particles										
	Killer defect density, D_pR_p (#/cm^2) [A]	**0.027**	**0.017**	**0.022**	**0.027**	**0.017**	**0.022**	**0.027**	**0.017**	**0.022**	*D ½*
	Critical particle diameter, d_c (nm) [B]	**40.1**	**35.7**	**31.8**	**28.4**	**25.3**	**22.5**	**20.1**	**17.9**	**15.9**	*D ½*
	Critical particle count, D_{pw} (#/wafer) [C]	**94.2**	**59.3**	**75.2**	**94.8**	**59.7**	**75.2**	**94.8**	**135.3**	**170.4**	*D ½*
	Back surface particle diameter: lithography and measurement tools (µm) [D][E]	**0.16**	**0.12**	**0.12**	**0.12**	**0.1**	**0.1**	**0.1**	**0.1**	**NA**	*D ½*
	Back surface particles: lithography and measurement tools (#/wafer) [D][E]	**400**	**400**	**200**	**200**	**200**	**200**	**200**	**200**	**NA**	*D ½*
	Back surface particle diameter: all other tools (µm) [D][E]	**0.2**	**0.16**	**0.16**	**0.16**	**0.14**	**0.14**	**0.14**	**0.14**	**NA**	*D ½*
	Back surface particles: all other tools (#/wafer) [D][E]	**400**	**400**	**200**	**200**	**200**	**200**	**200**	**200**	**NA**	*D ½*
	Critical GOI surface metals (10^{10} atoms/cm^2) [F]	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	*MPU*
	Critical other surface metals (10^{10} atoms/cm^2) [F]	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	*MPU*
	Mobile ions (10^{10} atoms/cm^2) [G]	**1.9**	**1.9**	**2**	**2.2**	**2.4**	**2.5**	**2.3**	**2.5**	**2.4**	*MPU*
	Surface carbon (10^{13} atoms/cm^2) [H]	**1.4**	**1.3**	**1.2**	**1**	**0.9**	**0.9**	**0.9**	**0.9**	**0.9**	
	Surface oxygen (10^{13} atoms/cm^2) [I]	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	**0.1**	*D ½, M*
	Surface roughness LVGX, RMS (Å) [J]	**4**	**4**	**4**	**4**	**4**	**2**	**2**	**2**	**2**	
WAS	Silicon loss (Å) per cleaning step [K]	**0.8**	**0.7**	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.2**	*M*
IS	Silicon loss (Å) per cleaning step [K]	**0.8**	**0.7**	**0.5**	**◆0.4**	**◆0.4**	**◆0.3**	**◆0.3**	**◆0.3**	**◆0.2**	
WAS	Oxide loss (Å) per cleaning step [L]	**0.8**	**0.7**	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.2**	*M*
IS	Oxide loss (Å) per cleaning step [L]	**0.8**	**0.7**	**0.5**	**◆0.4**	**◆0.4**	**◆0.3**	**◆0.3**	**◆0.3**	**◆0.2**	
	Allowable watermarks # [M]	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	*M*

Table 68b Surface Preparation Technology Requirements—Long-term Years UPDATED

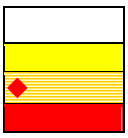
	Year of Production	2014	2015	2016	2017	2018	2019	2020	Driver
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14	D ½
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14	M
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6	M
	Wafer diameter (mm)	450	450	450	450	450	450	450	D ½, M
	Wafer edge exclusion (mm)	1.5	1.5	1.5	1.5	1.5	1.5	1.5	D ½, M
	Front surface particles								
	Killer defect density, D_pR_p (#/cm^2) [A]	0.027	0.017	0.022	0.027	0.017	0.022	0.027	D ½
	Critical particle diameter, d_c (nm) [B]	14.2	12.7	11.3	10.0	9.0	8.0	7.1	D ½
	Critical particle count, D_{pw} (#/wafer) [C]	214.6	135.4	170.5	214.6	135.4	170.4	214.9	D ½
	Back surface particle diameter: lithography and measurement tools (µm) [D][E]	NA	NA	NA	NA	NA	NA	NA	D ½
	Back surface particles: lithography and measurement tools (#/wafer) [D][E]	NA	NA	NA	NA	NA	NA	NA	D ½
	Back surface particle diameter: all other tools (µm) [D][E]	NA	NA	NA	NA	NA	NA	NA	D ½
	Back surface particles: all other tools (#/wafer) [D][E]	NA	NA	NA	NA	NA	NA	NA	D ½
	Critical GOI surface metals (10^{10} atoms/cm^2) [F]	0.5	0.5	0.5	0.5	0.5	0.5	0.5	MPU
	Critical other surface metals (10^{10} atoms/cm^2) [F]	1	1	1	1	1	1	1	MPU
	Mobile ions (10^{10} atoms/cm^2) [G]	2.4	2.3	2.3	2.3	2.3	2.3	2.3	MPU
	Surface carbon (10^{13} atoms/cm^2) [H]	0.9	0.9	0.9	0.9	0.9	0.9	0.9	
	Surface oxygen (10^{13} atoms/cm^2) [I]	0.1	0.1	0.1	0.1	0.1	0.1	0.1	D ½, M
	Surface roughness LVGX, RMS (Å) [J]	2	2	2	2	2	2	2	
WAS	Silicon loss (Å) per cleaning step [K]	0.2	0.2	0.2	0.2	0.2	0.2	0.2	M
IS	Silicon loss (Å) per cleaning step [K]	◆0.2	◆0.2	◆0.2	◆0.2	◆0.2	◆0.2	◆0.2	
WAS	Oxide loss (Å) per cleaning step [L]	0.2	0.2	0.2	0.2	0.2	0.2	0.2	M
IS	Oxide loss (Å) per cleaning step [L]	◆0.2	◆0.2	◆0.2	◆0.2	◆0.2	◆0.2	◆0.2	
	Allowable watermarks # [M]	0	0	0	0	0	0	0	M

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



Notes for Tables 68a and b:

[A] Killer defect density is calculated from the formula for 99% yield, $Y=0.99=\exp[-D_pR_pA_{eff}]$. A_{eff} is the effective chip area, D_p is the defect density, and R_p is a defect kill factor indicating the probability that a given defect will kill the device. The product D_pR_p is the density of device-killing defects on the wafer. R_p is dependent on numerous things including the size and shape of the particle, the composition of the particle, and specifics of the device layout. In previous years, R_p was assumed to be 0.2 for any particle > the critical particle size, d_c. For DRAM, $A_{eff}= 2.5F^2T+(1-aF^2T/A_{chip})*0.6A_{chip}$ where F is the minimum feature size, a is the cell fill factor, T is the number of DRAM bits (transistors) per chip, and A_{chip} is the DRAM chip size. For MPUs, $A_{eff}=aT(GL)^2$, where GL is the gate length. Because A_{eff} can increase or decrease with each successive technology generation, D_pR_p does not always decrease over time.

[B] Critical particle diameter, d_c, is defined by Yield Enhancement as ½ of the metal ½-pitch dimension. This should be considered an "effective" particle diameter as most particulate contamination is irregular in shape.

*[C] An example is provided which assumes that the kill factor, R_p, is 0.2 for all particles larger than the critical particle size. This is the assumption made in previous versions of the roadmap, but is not universally valid and is included only for purposes of an example calculation. Particles/wafer is calculated using [R_p*3.14159*(wafer radius-edge exclusion)^2]. To convert from particles/wafer at the critical particle size to particles/wafer at an alternative size, a suggested conversion formula is: $D_{alternate}=D_{critical}*(d_{critical}/d_{alternate})^2$.*

[D] and [E] These tables reflect particles added through touching the back surface of the wafer during processing and handling. For incoming wafers, the general consensus is that the specification of back surface particles should be the same as the front side (Table 68a). While there are some experimental models and empirical data available for particles added during process and handling (and future tables may use these models) there is, as yet, no industry agreement regarding the number or sizes of back surface particles that could be deleterious to semiconductor processing. Consequently, the back surface contact specs are based on present day realistic expectations (reflecting the TOTAL number of touches in any given front end of line process tool) and future aggressive lithographic improvements. Arguments have been made that back surface particles affect device yield mainly at the lithographic steps by causing the front surface of the wafer to move out of the focal plane leading to critical dimension variations. While it is not clear how the limited back surface contact achievable with pin chucks interacts with back surface particle density to cause front surface flatness variations, there is emerging evidence that "clustering" of small (<200 nm) particles are more likely to result in front side lithographic depth of focus problems than that of individual small particles. Because not all surface measurement tools are able to measure clustering, definitive data is not yet available, and future tables will reflect this data. In addition, it is also not clear how lithographic depth-of-focus (DOF) will change from year to year as this is not specified in the lithography roadmap. Aggressive specs for litho/measurement tool in outlying years (2007–2010) may necessitate edge-grip or edge-contact handling only. It is not possible to measure absolute levels of back surface particles on in-process wafers due to large variation in back surface finish and films especially for 200 mm wafers. A generally accepted practice is to process wafers with the polished front surface down in order to assess back surface particle adders for a particular process or operation. This metric reflects the TOTAL number of touches in any given front end of line process tool. Back surface particle metrics are for wafers with 3 mm edge exclusions as technology for measuring at/near the bevel edge is not available at this time. This limitation may be problematic for measuring particles generated by edge grip end-effectors.

[F] In roadmaps prior to 2003, metal contamination targets have been based on an empirically derived model predicting failure due to metal contamination as a function of gate oxide thickness. However, the oxides used in the experiments from which this model was derived were far thicker than gate oxide thicknesses used today. More recent data suggest an updated approach is appropriate. The metals are empirically grouped into three classes.[12, 13] *(a) Mobile metals which may be easily removed such as Na and K and may be modeled by taking the flat-band shift of a capacitance-voltage (CV) test less than or equal to 50 mV. (b) Metals which dissolve in silicon or form silicides such as Ni, Cu, Cr, Co, Hf, and Pt. (c) Major gate-oxide-integrity (GOI) killers such as Ca, Ba, and Sr. Metals such as Fe may fall into both classes (b) and (c). Targets for mobile ions are based on allowable threshold voltage shift from a CV test. Current targets for GOI killers and other metals are based on empirical data.*[14] *For extrapolation to future years, there may be reason to predict less stringent targets because effects should scale with respect to physical dielectric thickness (not EOT) that will increase upon introduction of high-κ gate dielectrics. However, in the absence of data to corroborate such a prediction, as well as predictions of physical dielectric thickness, the targets are left constant for future years. In addition, the introduction of SOI may also affect the allowable levels of metal contamination, as there is evidence metals may build up at the buried oxide layer interface. It is not yet clear how this will affect allowable metals level and has not been accounted for in these tables. Another factor to be considered in future years is the spatial distribution of localized contamination as opposed to the average contamination per wafer.*

[G] The model for mobile ions, D_i, calculates the number of ions that will create a threshold voltage shift that is within a portion of the Allowable Threshold Voltage Variability (ATVV). For the mobile ion model in 2005, it is assumed that the ATVV is 3% of the Nominal Power Supply Voltage for Low Operating Power or Low Standby Power Technology (see PIDS chapter). The portion of ATVV allocated to mobile ions is assumed to be 5%. Therefore, $D_i=1/q(C_{gate}*ATVV*0.05)$, where C_{gate} is computed for an electrically equivalent SiO_2 gate dielectric thickness and q is the charge of an electron. This model reduces to $D_i = ((3.9*8.85)/1.6)* (0.05*ATVV/EOT)*10^9$, where ATVV is in mV and EOT is in nm (also from Low Operating Power or Low Standby Power Technology Requirements Table in the PIDS chapter), and the oxide dielectric constant is 3.9. Note that the year-to-year value for D_i does not always decrease because D_i is not only proportional to ATVV, but is also inversely proportional to EOT.

[H] Residual carbon resulting from organic contamination after surface preparation. The original surface Carbon model was initiated at the 180 nm technology generation and corresponded to 10% carbon atom coverage of a bare silicon wafer (7.3E+13atoms/cm^2). Surface carbon for subsequent technology generations is scaled linearly with the ratio of CD (DRAM ½ pitch) to 180 nm. $D_C=(CD/180)(7.3E+13)$.

[I] Surface oxygen requirements at <1E+12 atoms/cm^2 are driven by the needs of pre-epitaxial cleaning. Epitaxial deposition of Si and SiGe is used for some devices, now, and will find more widespread use with the implementation of strained silicon channel technology. While some level of oxide can be removed in-situ, prior to epitaxial deposition, the trend towards lower deposition temperature will preclude the use of higher temperature hydrogen pre-bake processes. Surface oxygen concentrations up to <1E+13 atoms/cm^2 are acceptable for processes such as pre-silicide cleaning. Current pre-gate cleaning does not require an oxide-free surface, but the pre-gate surface should be either fully passivated by a continuous oxide layer or have <1E+13/cm^2. An intermediate level of oxygen will be unstable. Currently high-κ gate dielectrics require and oxide-passivated surfaces prior to deposition, however, much works is ongoing to be able to deposit high-κ dielectrics directly on silicon.

[J] In the 2001 ITRS, it was assumed channel mobility cannot be degraded by >10% due to surface preparation induced surface roughness. It was further claimed that current technologies were successfully manufactured with AFM based determination of 2Å RMS of surface micro-roughness. Where this is still approximately true for surface preparation induced, i.e. additive roughness, it is more direct to simply measure roughness on product immediately after the low voltage gate oxidation (LVGX) pre-clean. In this case, the total surface micro-roughness takes into account starting substrate roughness, plus the additional micro roughness induced by pre-cleans and strips of initial oxidation, any implant screen oxidations, or sacrificial oxidations, the first portions of the high voltage gate oxidation (dual gate flows), and any additional roughness brought about by plasma nitridations. With this taken into account, product has recently been successfully built with 4Å RMS surface micro-roughness. This may in part be explained by TCAD predictions that show carrier mobility being mainly affected by spatial frequencies smaller than those that are typically sampled by AFM micro-roughness metrology tools.

[K] The values for silicon loss are driven by requirements of high-performance Logic in the portion of the flow where source/drain extensions are fabricated. Specific values are relative to silicon loss measured optically on blanket polysilicon test wafers. Actual consumption on product will vary driven by damage from plasma etch/ash, ion implantation, and dopant concentrations. Decreasing values are in response to the requirement to control negative impact on drive currents (Ids). If the silicon under the source/drain extensions is recessed, this changes the junction profile increasing the source/drain extension resistance and decreasing drive currents. It is not yet possible to express a rigorous model connecting this metric with table parameters such as implant mask levels, junction depth, and critical dimension. IC manufacturers are currently targeting silicon loss to be 1.0Å per cleaning step for the 90 nm technology generation and 0.5Å per cleaning step for the 65 nm technology generation. It is not clear what will be required or possible in the longer term years, so the value is set at 0.4Å in 2008 and held constant until the 45 nm generation, then 0.3 Å until the 32 nm generation, then 0.2Å.

[L] The values for oxide consumption are driven by requirements of high-performance Logic in the portion of the flow where source/drain extensions are fabricated and tied to the silicon loss values. Specific values are relative to thermal oxide consumption on blanket test wafers. Actual consumption on product will vary driven by damage from plasma etch/ash, ion implantation, and dopant concentrations. Decreasing values are in response to the requirement to control negative impact on drive currents (Ids). If the silicon under the source/drain extensions is recessed, this changes the junction profile increasing the source/drain extension resistance and decreasing drive currents. By not consuming the oxide, assuming similar processing, this reduces the ability of subsequent processes to further oxidize and consume silicon. Less oxidized silicon equates to less silicon recess under the source/drain extensions. Also, consumption of deposited oxide in the isolation areas is a concern. It is not yet possible to express a rigorous model connecting this metric with table parameters such as implant mask levels, junction depth, and critical dimension. IC manufacturers are currently targeting oxide consumption to be 1.0Å per cleaning step for the 90 nm generation and 0.5Å per cleaning step for the 65 nm generation. It is not clear what will be required or possible in the longer term years, so the value is set at 0.4Å in 2008 and held constant until the 45 nm generation, then 0.3 Å until the 32 nm generation, then 0.2Å.

[M] Water marks cannot be tolerated on the wafer due to the catastrophic failure they cause on each die touched, as watermark can range from sub-micron to millimeters in diameter. Therefore a single wafer mark will exceed the maximum allowable die loss of 1%, hence the specification is zero water marks per wafer.

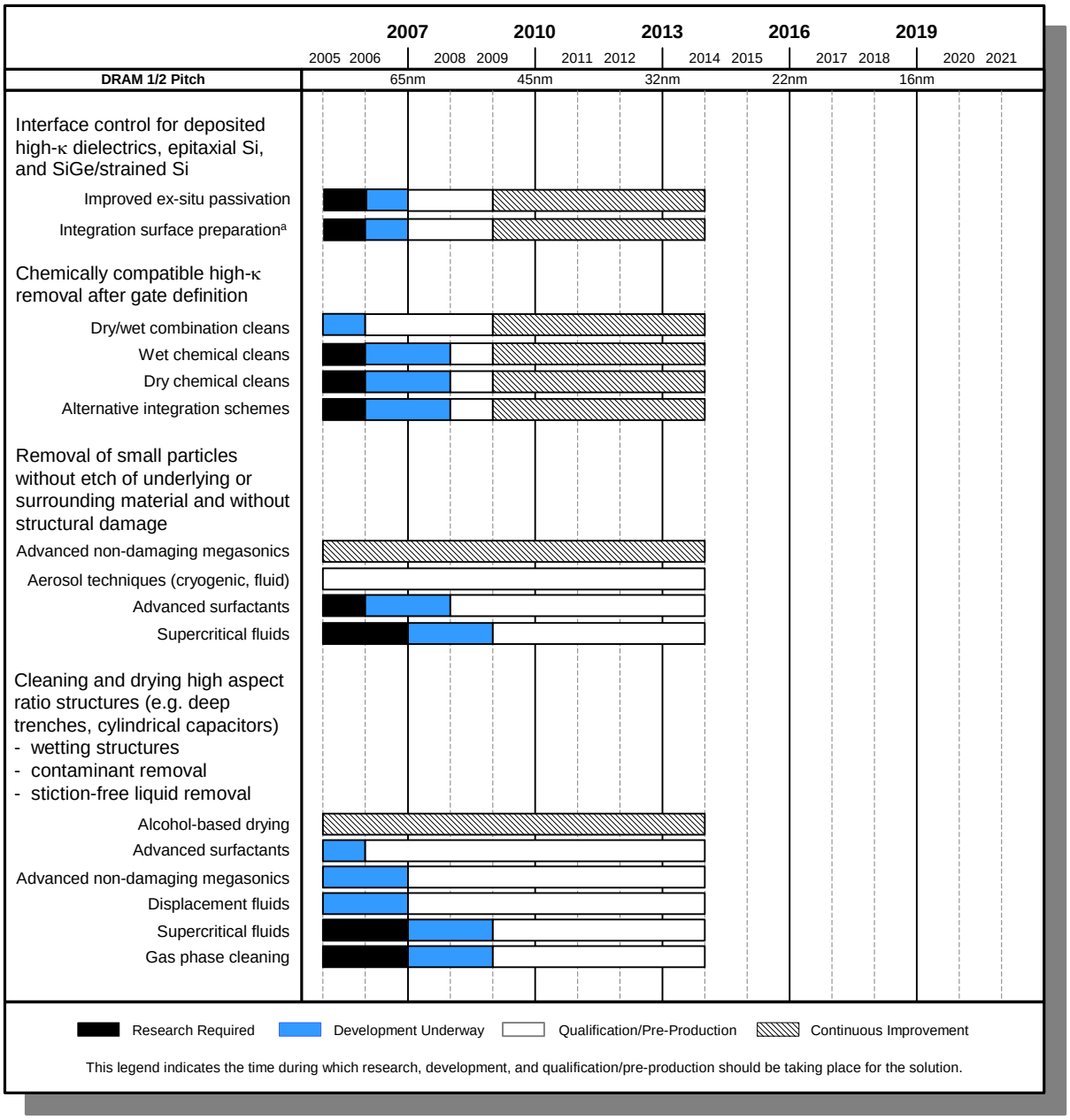


Figure 57 Surface Preparation Potential Solutions ***WAS***

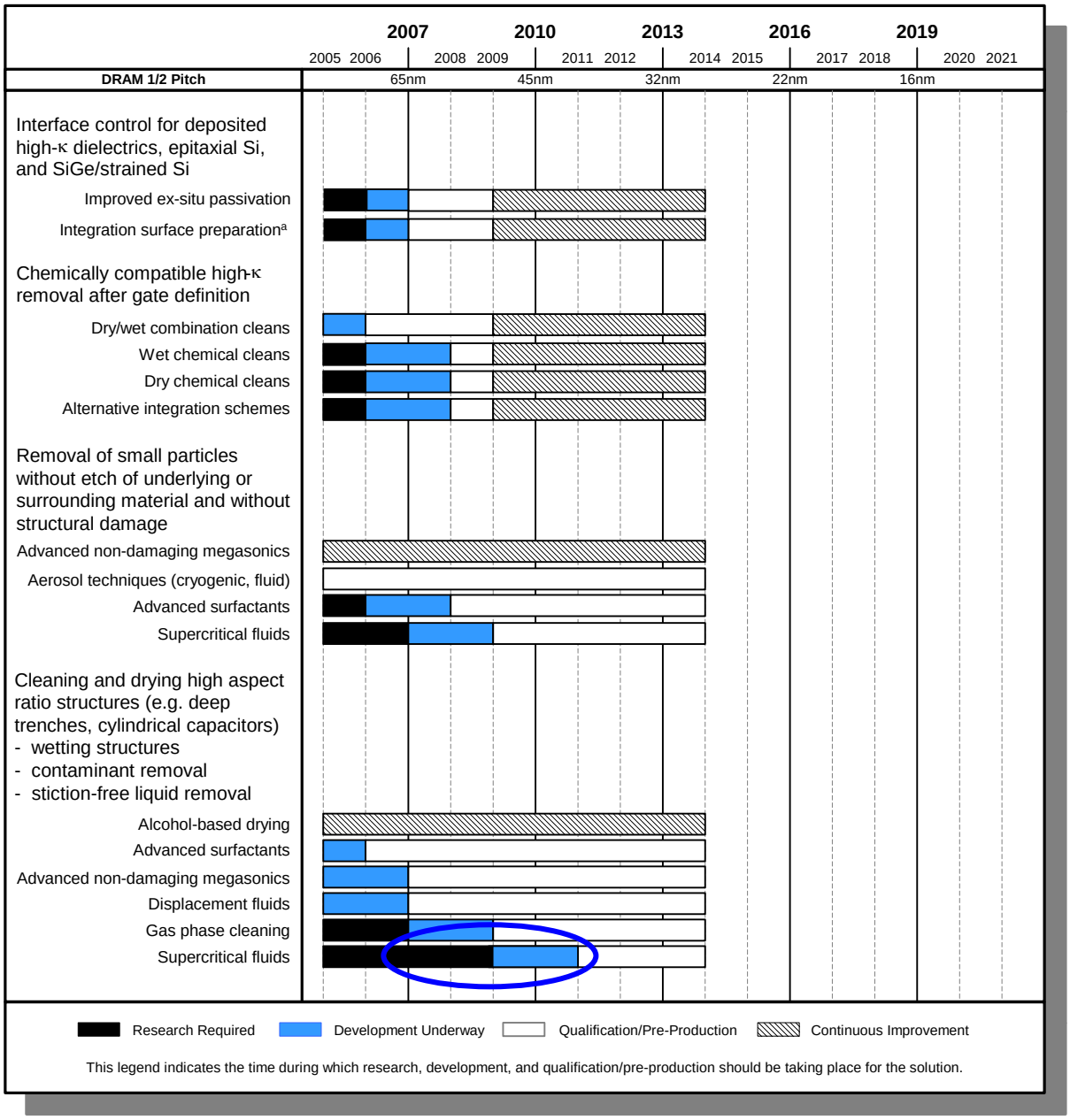


*Figure 57 Surface Preparation Potential Solutions **IS***

THERMAL/THIN FILMS, DOPING, AND ETCHING

Table 69a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term Years
UPDATED

Grey cells indicate the requirements projected only for near, intermediate, or long-term years.

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1E20-doped poly-Si [A, A1, A2]	1.1	1	1						
WAS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	1.2	1.1	1.1	0.5					
IS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	1.2	1.1	1.1	1	0.9				
WAS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 3E20-doped poly-Si [A, A1, A2]	1.3	1.2	1.2	0.71	0.54	0.41			
IS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for 3E20-doped poly-Si [A, A1, A2]	1.3	1.2	1.2	1.2	1.1	0.41			
WAS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]				0.9	0.75	0.65	0.5	0.5	
IS	Equivalent physical oxide thickness for bulk MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]				~~0.9~~	~~0.75~~	0.65	0.5	0.5	
WAS	Gate dielectric leakage at 100 °C (A/cm^2) bulk high-performance [B, B1, B2]	1.80E+02	5.40E+02	8.00E+02	9.10E+02	1.10E+03	1.60E+03	2.00E+03	2.40E+03	
IS	Gate dielectric leakage at 100 °C (A/cm^2) bulk high-performance [B, B1, B2]	1.80E+02	5.40E+02	8.00E+02	1.20E+03	1.10E+03	1.60E+03	2.00E+03	2.40E+03	
WAS	Metal gate work function for bulk MPU/ASIC $\lvert E_{c,v} - \phi_m \rvert$ (eV) [C]				<0.2	<0.2	<0.2	<0.2	<0.2	
IS	Metal gate work function for bulk MPU/ASIC $\lvert E_{c,v} - \phi_m \rvert$ (eV) [C]				~~<0.2~~	~~<0.2~~	<0.2	<0.2	<0.2	
WAS	Channel doping concentration (cm^{-3}), for bulk design [D]	3.70E+18	4.60E+18	5.40E+18	7.30E+18	8.60E+18	8.90E+18	8.60E+18	8.80E+18	
IS	Channel doping concentration (cm^{-3}), for bulk design [D]	3.25E+18	3.68E+18	4.19E+18	5.80E+18	7.30E+18	7.14E+18	8.08E+18	9.00E+18	
	Bulk/FDSOI/DG – Long channel electron mobility enhancement factor for MPU/ASIC [E]	1.7	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
	Drain extension X_j (nm) for bulk MPU/ASIC [F]	11	9	7.5	7.5	7	6.5	5.8	4.5	
	Maximum allowable parasitic series resistance for bulk NMOS MPU/ASIC × width (Ω–μm) [G]	180	170	140	140	120	105	80	70	
	Maximum drain extension sheet resistance for bulk MPU/ASIC (NMOS) (Ω/sq) [G]	653	674	640	740	677	650	548	593	
	Extension lateral abruptness for bulk MPU/ASIC (nm/decade) [H]	3.5	3.1	2.8	2.5	2.2	2	1.8	1.5	
	Contact X_j (nm) for bulk MPU/ASIC [I]	35.2	30.8	27.5	25.3	22	19.8	17.6	15.4	

16 Front End Processes

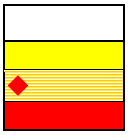
	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	Allowable junction leakage for bulk MPU/ASIC ($\mu A/\mu m$)	0.06	0.15	0.2	0.2	0.22	0.28	0.32	0.34	
	Sidewall spacer thickness (nm) for bulk MPU/ASIC [J]	35.2	30.8	27.5	25.3	22	19.8	17.6	15.4	
	Maximum silicon consumption for bulk MPU/ASIC (nm) [K]	17.6	15.4	13.8	12.7	11	9.9	8.8	7.7	
	Silicide thickness for bulk MPU/ASIC (nm) [L]	21	19	17	15	13	12	11	9	
	Contact silicide sheet R_s for bulk MPU/ASIC (Ω/sq) [M]	7.5	8.6	9.6	10.5	12.1	13.5	15.1	17.3	
	Contact maximum resistivity for bulk MPU/ASIC (Ω-cm^2) [N]	1.60E-07	1.30E-07	9.50E-08	8.30E-08	6.20E-08	4.70E-08	3.20E-08	2.50E-08	
	STI depth bulk (nm) [O]	367	359	353	339	335	331	323	316	
	Trench width at top (nm) [P]	80	70	65	57	50	45	40	35	
	Trench sidewall angle (degrees) [Q]	>86.9	>87.2	>87.4	>87.6	>87.9	>88.1	>88.2	>88.4	
	Trench fill aspect ratio – bulk [R]	5.1	5.6	5.9	6.4	7.2	7.9	8.6	9.5	
WAS	Equivalent physical oxide thickness for FDSOI MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]				0.9	0.8	0.7	0.6	0.5	0.5
IS	Equivalent physical oxide thickness for FDSOI MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]				~~0.9~~	~~0.8~~	0.7	0.6	0.5	0.5
WAS	Gate dielectric leakage at 100°C (A/cm^2) FDSOI high-performance [B, B1, B2]				7.70E+02	9.50E+02	1.20E+03	1.40E+03	2.10E+03	2.20E+03
IS	Gate dielectric leakage at 100°C (A/cm^2) FDSOI high-performance [B, B1, B2]				~~7.70E+02~~	~~9.50E+02~~	1.20E+03	1.40E+03	2.10E+03	2.20E+03
WAS	Metal gate work function for FDSOI MPU/ASIC $\phi_m - E_i$ (eV) NMOS/PMOS [S]				+/– 0.15	+/– 0.15	+/– 0.15	+/– 0.15	+/– 0.15	+/– 0.15
IS	Metal gate work function for FDSOI MPU/ASIC $\phi_m - E_i$ (eV) NMOS/PMOS [S]				~~+/– 0.15~~	~~+/– 0.15~~	+/– 0.15	+/– 0.15	+/– 0.15	+/– 0.15
	Saturation velocity enhancement factor MPU/ASIC [T]	1	1	1	1.1	1.1	1.1	1*	1*	1*
WAS	Si thickness FDSOI (nm) [U]				7.6	6.8	6.2	5.4	5.1	4.4
IS	Si thickness FDSOI (nm) [U]				~~7.6~~	~~6.8~~	6.2	5.4	5.1	4.4
WAS	Maximum allowable parasitic series resistance for FDSOI NMOS MPU/ASIC × width (Ω–μm) [G]				155	140	125	110	90	75
IS	Maximum allowable parasitic series resistance for FDSOI NMOS MPU/ASIC × width (Ω–μm) [G]				~~155~~	~~140~~	125	110	90	75
WAS	Maximum drain extension sheet resistance for FDSOI MPU/ASIC (NMOS) (Ω/sq) [G]				688	691	679	682	649	628
IS	Maximum drain extension sheet resistance for FDSOI MPU/ASIC (NMOS) (Ω/sq) [G]				~~688~~	~~691~~	679	682	649	628
WAS	Spacer thickness, FDSOI elevated contact [J]				12.1	11	9.9	8.8	7.7	7.2
IS	Spacer thickness, FDSOI elevated contact [J]				~~12.1~~	~~11~~	9.9	8.8	7.7	7.2
WAS	Thickness of FDSOI elevated junction (nm) [V]				22	20	18	16	14	13
IS	Thickness of FDSOI elevated junction (nm) [V]				~~22~~	~~20~~	18	16	14	13

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
WAS	Maximum silicon consumption for FDSOI MPU/ASIC (nm) [K]				22	20	18	16	14	13
IS	Maximum silicon consumption for FDSOI MPU/ASIC (nm) [K]				~~22~~	~~20~~	18	16	14	13
WAS	Silicide thickness for FDSOI MPU/ASIC (nm) [L]				28	24	22	19	17	16
IS	Silicide thickness for FDSOI MPU/ASIC (nm) [L]				~~28~~	~~24~~	22	19	17	16
WAS	Contact silicide sheet R_s for FDSOI MPU/ASIC (Ω/sq) [M]				5.8	6.7	7.4	8.3	9.5	10.2
IS	Contact silicide sheet R_s for FDSOI MPU/ASIC (Ω/sq) [M]				~~5.8~~	~~6.7~~	7.4	8.3	9.5	10.2
WAS	Contact maximum resistivity for FDSOI MPU/ASIC (Ω-cm^2) [N]				9.00E-08	7E0-8	6.00E-08	4.00E-08	3.00E-08	2.00E-08
IS	Contact maximum resistivity for FDSOI MPU/ASIC (Ω-cm^2) [N]				~~9.00E-08~~	~~7E0-8~~	6.00E-08	4.00E-08	3.00E-08	2.00E-08
	Trench fill aspect ratio – FDSOI [W]				0.6	0.6	0.6	0.6	0.6	0.6
	Equivalent physical oxide thickness for multi-gate MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]							0.8	0.7	0.6
	Gate dielectric leakage at 100°C (nA/μm) muti-gate high-performance [B, B1, B2]							6.30E+02	7.90E+02	8.50E+02
	Metal gate work function for multi-gate MPU/ASIC [S]							midgap	midgap	midgap
	Si thickness for multi-gate (nm) [U]							10.3	9	8.4
	Maximum allowable parasitic series resistance for multi-gate NMOS MPU/ASIC × width (Ω–μm) [G]							105	95	90
	Maximum drain extension sheet resistance for multi-gate MPU/ASIC (NMOS) (Ω/sq) [G]							543	557	565
	Spacer thickness, multi-gate elevated contact [J]							8.8	7.7	7.2
	Thickness of multi-gate elevated junction (nm) [V]							16	14	13
	Maximum silicon consumption for multi-gate MPU/ASIC (nm) [K]							16	14	13
	Silicide thickness for multi-gate MPU/ASIC (nm) [L]							19	17	16
	Contact silicide sheet R_s for multi-gate MPU/ASIC (Ω/sq) [M]							8.3	9.5	10.2
	Contact maximum resistivity for multi-gate MPU/ASIC (Ω-cm^2) [N]							4.20E-08	3.40E-08	2.90E-08
	Physical gate length low operating power (LOP) (nm)	45	37	32	28	25	23	20	18	16
WAS	Equivalent physical oxide thickness for bulk low operating power T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	1.4	1.3	1.2	0.8	0.7	0.6	0.6	0.6	
IS	Equivalent physical oxide thickness for bulk low operating power T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	1.4	1.3	1.2	1.1	1	0.6	0.6	0.6	

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
WAS	Equivalent physical oxide thickness for bulk low operating power T_{ox} (nm) for metal gate [A, A1, A2]				1.1	1	0.9	0.9	0.9	
IS	Equivalent physical oxide thickness for bulk low operating power T_{ox} (nm) for metal gate [A, A1, A2]				~~1.1~~	~~1~~	0.9	0.9	0.9	
WAS	Gate dielectric leakage at 100°C for bulk (A/cm^2) LOP [B, B1, B2]	3.30E+01	4.10E+01	7.80E+01	8.90E+01	1.00E+02	1.10E+02	4.50E+02	6.90E+02	
IS	Gate dielectric leakage at 100°C for bulk (A/cm^2) LOP [B, B1, B2]	3.30E+01	4.10E+01	7.80E+01	9.80E+01	1.70E+02	1.10E+02	4.50E+02	6.90E+02	
WAS	Metal gate work function for bulk low operating power $\|E_{c,v} - \phi_m\|$ (eV) [S]				<0.2	<0.2	<0.2	<0.2	<0.2	
IS	Metal gate work function for bulk low operating power $\|E_{c,v} - \phi_m\|$ (eV) [S]				~~<0.2~~	~~<0.2~~	<0.2	<0.2	<0.2	
	Allowable junction leakage for bulk LSTP (pA/μm)	10	10	10	10	10	10	16	21	
	Equivalent physical oxide thickness for FDSOI low operating power T_{ox} (nm) for metal gate [A, A1, A2]							0.9	0.9	0.8
	Gate dielectric leakage at 100°C for FDSOI (A/cm^2) LOP [B, B1, B2]							2.00E+02	2.80E+02	3.10E+02
	Metal gate work function for FDSOI and multi-gate LOP [S]							midgap	midgap	midgap
	Equivalent physical oxide thickness for multi-gate low operating power T_{ox} (nm) for metal gate [A, A1, A2]							0.9	0.9	0.8
	Gate dielectric leakage at 100°C for multi-gate (A/cm^2) LOP [B, B1, B2]							1.30E+02	1.90E+02	2.20E+02
	Physical gate length low standby power (LSTP) (nm)	65	53	45	37	32	28	25	23	20
	Equivalent physical oxide thickness for bulk low standby power T_{ox} (nm) for 1.5E20-doped poly-Si [A, A1, A2]	2.1	2	1.9	1.2	1.1	1	1	0.9	0.8
	Equivalent physical oxide thickness for bulk low standby power T_{ox} (nm) for metal gate [A, A1, A2]				1.6	1.5	1.4	1.4	1.3	1.2
	Gate dielectric leakage at 100°C for bulk (A/cm^2) LSTP [B, B1, B2]	1.50E-02	1.90E-02	2.20E-02	2.70E-02	3.10E-02	3.60E-02	4.80E-02	7.30E-02	1.10E-01
	Metal gate work function for bulk LSTP $\|E_{c,v} - \phi_m\|$ (eV) [S]				<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
	Equivalent physical oxide thickness for FDSOI low standby power T_{ox} (nm) for metal gate [A, A1, A2]								1.3	1.2
	Gate dielectric leakage at 100°C for FDSOI (A/cm^2) LSTP [B, B1, B2]								4.50E-02	5.00E-02
	Metal gate work function for FDSOI and multi-gate LSTP $\phi_m - E_i$ (eV) NMOS/PMOS [S]								-/+ 0.1	-/+ 0.1

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Equivalent physical oxide thickness for multi-gate low standby power T_{ox} (nm) for metal gate [A, A1, A2]								1.2	1.1
Gate dielectric leakage at 100°C for multi-gate (A/cm^2) LSTP [B, B1, B2]								4.50E-02	5.00E-02
Thickness control EOT (% 3σ) [X]	<±4	<±4	<±4	<±4	<±4	<±4	<±4	<±4	<±4
Poly-Si or metal gate electrode thickness (approximate) (nm) [Y]	64	56	50	46	40	36	32	28	26
Gate etch bias (nm) [Z]	22	20	17	15	14	12	11	10	8
L_{gate} 3σ variation (nm) [AA]	3.84	3.36	3	2.76	2.4	2.16	1.92	1.68	1.56
Total maximum allowable lithography 3σ (nm) [AB]	3.33	2.91	2.6	2.39	2.08	1.87	1.66	1.45	1.35
Total maximum allowable etch 3σ (nm), including photoresist trim and gate etch [AB]	1.92	1.68	1.5	1.38	1.2	1.08	0.96	0.84	0.78
Resist trim maximum allowable 3σ (nm) [AC]	1.11	0.97	0.87	0.8	0.69	0.62	0.55	0.48	0.45
Gate etch maximum allowable 3σ (nm) [AC]	1.57	1.37	1.22	1.13	0.98	0.88	0.78	0.69	0.64
CD bias between dense and isolated lines [AD]	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%
Minimum measurable gate dielectric remaining (post gate etch clean) [AE]	>0	>0	>0	>0	>0	>0	>0	>0	>0
Profile control (side wall angle) [AF]	90	90	90	90	90	90	90	90	90
Allowable V_t shift from charge in dielectric (mV) [AG]	10	10	10	10	10	10	10	10	10
Allowable interfacial charge in high-κ gate stack (cm^{-2})[AH]	1.00E+11	1.10E+11	1.10E+11	1.80E+11	2.00E+11	2.20E+11	2.20E+11	2.40E+11	2.70E+11
Allowable bulk charge in high-κ gate stack (cm^{-3}) [AI]	2.40E+17	2.70E+17	3.00E+17	7.50E+17	8.90E+17	1.10E+18	1.10E+18	1.30E+18	1.70E+18
Allowable bulk charge in high-κ gate stack (ppm) [AI]	11.1	12.3	13.6	34	40.5	49	49	60.5	76.6
Allowable critical metal impurity level in high-κ dielectric (ppm) [AJ]	1.1	1.2	1.4	3.4	4.1	4.9	4.9	6.1	7.7

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 69a and b UPDATED

[A] This number represents the effective thickness of the dielectric alone, at the maximum operating frequency of the technology, without substrate or electrode effects. This parameter is obtained through an electrical measurement of capacitance corrected for substrate (quantum) and electrode (depletion) effects. The electrical, or capacitance equivalent, thickness (CET), in contrast to EOT, includes a contribution due to gate (Poly-Si) depletion. A more detailed discussion of the measurement of EOT is on a separate workbook page of the linked file . Values for EOT were derived from the electrical device requirements (CET) as given in the PIDS chapter. MASTAR and other simulations were used to subtract the substrate dark space and gate depletion for the prescribed channel configuration, doping and voltage at each technology generation.

[A1] EOT values are reported for alternate gate electrode options: Poly-Si whose doping at the dielectric interface is $1 \times 10^{20}/cm^3$ (light doping), $1.5 \times 10^{20}/cm^3$ (the nominal case) and $3 \times 10^{20}/cm^3$ (representing aggressive doping) and Metal gate. In approximate terms, Poly depletion for 1.5E20 doping was about 0.4 nm, and it was about 0.3 nm for 3e20. Thus, increasing Poly-Si doping from 1E20 to 3E20 increases the allowable EOT by 0.2 nm. Similarly, metal gates can use EOTs that are about 0.4 nm thicker than 1.5E20-doped Poly-Si. Due to numerous practical difficulties at the high-κ/Poly-Si interface, it is envisioned that many companies may want to introduce metal gate at the same time, or maybe even before, high-κ dielectrics are introduced.

WAS *[A2] The color-coding of each technology generation considers the ability of known dielectrics to meet gate leakage, uniformity, and reliability requirements. For all three applications (HP, LOP, and LSTP), the gate leakage requirements, in this scenario, can no longer be met by optimized oxynitride (which is taken to have a leakage of 1/30 that of SiO_2); hence high-κ dielectric is needed. Based on early announcements and encouraging results with high-κ dielectrics and poly-Si gates, particularly at 1 nm EOT and above, (many of which employed a layered SiON-HfSiON system), were colored yellow. All other high-κ dielectrics, i.e., those thinner than 1 nm and those requiring metal gates, are colored red because a manufacturing solution to all known problems is not at hand.*

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WAS *[B] The gate leakage, specified at 100°C, is derived from the transistor sub-threshold leakage at room temperature. This device leakage is specified in the PIDS chapter section on Logic—High Performance and Low Power Technology Requirements as the off-state leakage (excluding the junction and the gate leakage components) at room temperature. The gate leakage specification (at 100°C) is taken to be multiple of the (room temperature) device sub-threshold leakage spec. The multiplier includes two factors: The first, or Initial Factor, accounts for the fact that not all transistors on real chips are not the low V_t (high leakage but high current drive; hence, fast) transistors specified in the PIDS table. Most transistors on HP chips are higher V_t, lower leakage and current drive. The factor of 0.1 is our estimate of a reasonable number to use to take account of these multiple transistor in HP. Conversely in LOP and LSTP chips, most of the devices are the lower V_t; hence the initial factor is 1. The second factor, High T Factor, is used to account for the fact that the device sub-threshold leakage, which is specified at room temperature, rapidly increases with operating temperature. For high-performance devices, which operate at high temperatures, this factor was taken as 10; for low operating and low standby power applications, where the temperature is lower, the factors were taken as 5 and 1, respectively. Models are provided online as linked supplemental files, in the electronic version of this chapter at http://public.itrs.net. Tying the gate leakage to the device sub-threshold leakage in this way was assumed to be satisfactory from a circuit's operation standpoint, but it should be noted that not all design approaches (companies) will allow such a high gate leakage. The gate leakage is measured on the minimum nominal device, and the specification is taken to apply to all transistor bias configurations, that is, both when $V_g = V_s = 0$ and $V_d = V_{dd}$ as well as when $V_s = V_d \approx 0$ and $V_g = V_{dd}$.*

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[B1] The areal gate leakage is modeled as the allowable gate leakage divided by the physical gate length. However, it should be noted that the total gate leakage is the sum of three leakage components: 1) leakage between the source and the gate in the gate-source overlap area, 2) leakage between the channel and the gate over the channel region, and 3) leakage between the gate and the drain in the gate-drain overlap area. The magnitude of each of these three components will depend on the gate, source, and drain biasing conditions. The color coding of leakage values is based on UTQUANT simulations of tunneling current from an inversion channel to the gate for the mid-point EOT. (These simulation results are given in a separate worksheet file online at http://public.itrs.net.) It should be emphasized that the tunneling current density will generally be much higher between the junction and gate than between an inversion channel and gate. Thus these simulations represent a best case (lowest leakage) condition, where the gate-to-junction overlap area is minimal. When oxide will meet the leakage specification, the value is coded white. Based on recent experience, optimized oxynitride dielectrics have about 30 times less leakage current than oxide; value are coded white when optimized oxynitride is needed to meet the leakage specs. Requirement values requiring alternate, high-κ dielectrics are coded yellow or red as discussed in Footnote A2.

[B2] The unmanaged gate leakage power is the total static chip power that would occur if all the devices on a chip had gate leakage equal to the maximum allowable value. Power management will require the extensive use of power reduction techniques, such as power-down or multiple V_t devices to achieve an acceptable static power level.

[C] The gate electrode work functions come from the PIDS device design. In bulk devices, the electrode work function and the channel doping jointly control device threshold, which is selected to maximize I_{on}, while meeting the I_{off} specification. In addition, the doping affects both short channel effects and channel mobility and, thus, requires an optimization. The PIDS design shows that work functions 0.1 eV below E_c and 0.1 eV above E_v are best for NMOS and PMOS respectively. The requirement stated in the table is for the work function to be within 0.2 eV of the Silicon band edge. Even though there is some leeway in the choice of the gate work functions, the work function itself needs to be controlled to within about 10 mV 3σ, since that it becomes a component of the device threshold voltage tolerance.

[D] The channel doping for bulk CMOS devices comes from the PIDS device design. The doping, along with the gate dielectric thickness and the junction depth control short channel effects and thus must be co-optimized. The reduced short channel effects associated with higher channel doping must also be traded off for reduced channel mobility and increased tunnel leakage. The values presented in the table reflect a representative co-optimization. Channel doping above $5 \times 10^{18}/cm^3$ was colored yellow because of concerns about excessive band-to-band tunneling leakage in junctions.

[E] Bulk/FDSOI/DG – Long channel Electron Mobility Enhancement Factor, representing the enhancement in peak electron mobility in NMOS devices.

WAS

*[F] X_j at Channel (Extension Junction) as given by the PIDS Bulk device designs (with a range of ± 25%). In earlier roadmaps X_j was taken as 0.55*Physical Gate Length; however since CET is no longer scaling with gate length, extension junction scaling has become more aggressive. Junction depths for NMOS and PMOS are the same.*

IS

*[F] X_j at Channel (Extension Junction) as given by the PIDS Bulk device designs (with a range of ± 25%). In earlier roadmaps X_j was taken as 0.55*Physical Gate Length; however since CET is no longer scaling with gate length, extension junction scaling has become* ***much*** *more aggressive.* ***Alternative device designs, employing offset spacers and deeper extension junctions which preserve or even extend the effective channel length, may allow deeper extension junctions. A more comprehensive analysis will be performed in 2007.*** *Junction depths for NMOS and PMOS are the same.*

[G] The maximum allowable parasitic series resistance for NMOS devices comes from the PIDS device design. The allowable resistance for PMOS is taken to be 2.2 times the NMOS values. The maximum drain extension sheet resistance is modeled by allocating 15% of the allowable source and drain parasitic resistances to the drain extensions. (See the worksheet labeled R_sX_j in the linked file of the electronic version of this chapter, online at http://public.itrs.net). The drain extension sheet resistance value must be optimized together with the contact resistance and junction lateral abruptness (which effects spreading resistance), in order to meet the overall parasitic resistance requirements. This is a relatively crude model and the resultant sheet resistance values should only be used as a guide.

*[H] Channel abruptness in nm per decade drop-off in doping concentration) = 0.11 * Physical Gate Length (nm – based on Short Channel effect.[15] This lateral abruptness is consistent with a 3 decade fall off of doping over the lateral extent of the junction, which is taken to be 60% of the vertical junction depth. Note discussion of the integration choices in the supplemental material online at http://public.itrs.net.*

*[I] Contact Junction Depth = 1.1*Physical Gate Length (with a range of ±33%) for Bulk devices. Junction depths for NMOS and PMOS are the same.*

[J] Spacer thickness (width) is taken as the same as the Contact Junction Depth, namely $1.1 \times L_{gate}$,, for bulk devices.. Validity established using response surface methodology in "Response Surface Based Optimization of 0.1 μm PMOSFETs with Ultra-Thin Oxide Dielectrics"[16]. For FDSOI and Multi-gate devices, the spacer width was taken to be half that value, i.e., $0.55 \times L_{gate}$. (See the worksheet labeled R_sX_j in the linked file of the electronic version of this chapter, online at http://public.itrs.net).

[K] Silicon consumption is based on half the contact junction depth, for bulk devices. For advanced fully depleted and multi-gate devices, having elevated contacts, the silicide thickness is such that the silicide/silicon interface is coplanar with the channel/gate dielectric interface. The silicon consumption is equal to the added silicon thickness.

[L] Silicide thickness is based on the silicon consumption, which is taken to be 1/2 of the Contact X_j midpoint to avoid consumption-induced increase in contact leakage for bulk devices. Less than half of the junction can be consumed.[17] For fully-depleted and multi-gate devices, having elevated contact structures, the silicide thickness is that thickness yielded by consumption of the contact silicon added above the plane of the gate dielectric/channel interface. For cobalt and titanium di-silicide layers this silicide thickness is nominally equal to the silicon consumed. For nickel mono-silicide the silicide thickness is equal to 2.22/1.84× of the silicon consumed. In the table we have assumed NiSi implementation. (See the worksheet labeled R_sX_j in the linked file of the electronic version of this chapter, online at http://public.itrs.net).

[M] Contact silicide sheet resistance: assumes 16 μΩ-cm silicide resistivity for NiSi.

[N] The Si/Silicide maximum interfacial contact resistivity values were calculated assuming that 100% of the PIDS total allowed MOSFET Source/Drain resistance is allocated to the contact resistivity. It further assumes that the transistor contact length is taken to be twice the MPU half pitch, where length is in the direction of current flow. Since the PIDS allocation is in terms of $R_s \times W$, the equation for the contact resistivity rhoc is: $rhoc = R_s \times W \times M$. These values should be appropriately modified if different transistor contact lengths are assumed. (See the worksheet on Contact Rs in the linked file of the electronic version of the chapter online at http://public.itrs.net). Note that this contact resistivity is the maximum allowable and cannot be used for real devices. The contact resistivity was colored red below 9×10^{-8} Ohm-cm^2 and white above 1×10^{-7} Ohm-cm^2. The values of contact resistivity, drain extension sheet resistance, and drain extension lateral abruptness must be co-optimized in order to meet the overall parasitic resistance requirements.

[O] Assumes that the trench depth for bulk is proportional to the contact junction depth plus depletion width into the well. The constant of proportionality was determined by setting the 2003 value equal to 400 nm.

[P] Assumes a minimum trench width equal to the MPU half-pitch.

[Q] Assumes that the trench width is reduced by no more than half of the top dimension.

[R] Assumes a mask thickness equal to half of the DRAM half-pitch adds to the trench depth in the substrate

[S] In fully-depleted and multi-gate devices, the gate work function is the prime determinant of device threshold; accordingly values near midgap are more appropriate. The scenario depicted in the table is one which seeks to maintain the same work function over time for a given device type and to minimize the number of different work functions needed for different applications. Dual work function gates are best served with work functions that are ± 0.15 eV from midgap for NMOS and PMOS respectively (± 0.1 eV for LSTP applications). Several applications, including some low cost ones, can be satisfied with a single midgap work function for both NMOS and PMOS. As with gate electrodes for bulk devices, work function control of 10 mV, 3σ is required.

*[T] Saturation Velocity enhancement factor. *After 2013, a velocity enhancement factor is included into the Ballistic enhancement factor, k_{bal} (see PIDS chapter)*

[U] Si thicknesses for FDSOI and multi-gate devices was based on PIDS device optimization to control short channel effects. Although some company-to-company differences in the final optimized nominal thickness is expected, the tolerance on the final thickness is ±10%. The colorization of the FDSOI thickness is based on thinning the material specified in the Starting Materials tables (in Tables 68a and b), which are controlled to ±5%, to the final thicknesses required by PIDS devices, which require a ±10% tolerance, assuming that the thinning process introduces no additional variation in thickness. Silicon thickness for all multi-gate requirements was colored red, where control of the thickness, sidewall angle, and channel mobility have not been demonstrated.

[V] The thickness of the elevated junctions in FDSOI and in Multi-gate was taken as equal to the Physical Gate Length. In this model, the entire thickness of the elevated junction is consumed to form silicide. By adjusting this thickness tradeoffs can be made between silicide sheet resistance and lateral parasitic junction-to-gate capacitance.

[W] Based on a trench depth equal to the FDSOI thickness

[X] From Modeling of Manufacturing Sensitivity and of Statistically Based Process Control [18] Requirements for 0.18 micron NMOS device.

[Y] Gate thickness is taken as two times the physical gate length. Thicker gates reduce gate series resistance, but at the expense of increased topography and aspect ratio.

[Z] Bias is defined as the difference between the printed gate length and the final post-etch gate length.

[AA] The total gate length 3σ variation encompasses all random process variation including point-to-point on a wafer, wafer-to-wafer, and lot-to-lot variations. It excludes systematic variations such as lithography proximity effects, and etch variations such as CD bias between densely spaced and isolated lines. This total variability is taken to be less than or equal to 12% of the final feature size. A conventional MOS structure is the basis for these calculations. MOS transistor structures that vary in any way from the conventional structure (e.g. Vertical MOS transistors) will have different technical challenges and will not fall within these calculations. The data is computed taking into account lithographic errors during resist patterning and combined etch errors due to both resist trim and gate etch.

[AB] The allowable lithography variance σ^2_L is limited to 3/4 of the total variance, σ^2_T of the combined lithography and etch processes. It is further assumed that the lithographic and etch processes are statistically independent and therefore that the total variance is the sum of the etch and lithography variances. This implies among other things that the printed features in the resist have vertical wall profiles and be sufficiently thick to with-stand the etch process without loss of dimensional fidelity. Refer to the Etch supplemental file in the electronic version of this chapter online at http://public.itrs.net.

[AC] It is assumed that the resist trim and gate etch processes are statistically independent and therefore that the respective variances, σ^2, of the two processes are additive. 1/3 of the combined trim-etch variance is allocated to the trim process, with the remaining 2/3 allocated to the etch process.

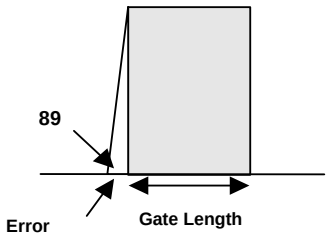
[AD] 15% dense-iso CD budget is a combination of measurements from Etch, Lithography and Metrology.

[AE] It is important that some dielectric remains after the gate etch clean step. Between technology generations the dielectric thickness decreases and there is an onset of using high-κ materials (2008) to replace the gate dielectric. Both advances represent challenges to ensure there is an amount of remaining dielectric and the ability to measure the remaining material.

[AF] Profile can be a major contributor to etch errors (see inset). Accurate measurement of vertical profiles remains difficult. Long term, the effect of edge roughness on device performance needs to be addressed and methodology of the measurement determined.

Gate error produced @ 89 degrees = 3.5 nm

Gate Length:	65nm	53nm	45nm	37nm	32nm	30nm	25nm
% error =	5.4	6.6	7.8	9.4	10.9	11.7	14



[AG] Values taken from SEMATECH working documents. Charge includes centers that are initially charges or centers which trap/detrap charge during long term stressing.

[AH] Assumes that all of the charge is at the Si-gate dielectric interface, i.e., there is no bulk charge and no charge at an SiO_2/high-κ interface

[AI] Assumes: i) a single (high-κ) dielectric with uniformly-distributed charge, and ii) a relative dielectric constant of 4 times that of SiO_2. Conversion of the bulk concentrations to units of ppm in the dielectric assume the metal atom density in the high-κ dielectric is the same as that of Si in SiO_2, namely $2.2 \times 10^{22}/cm^3$.

[AJ] Assumes that 90% of the charge (and traps) in the high-κ are due to intrinsic bonding defects and that 10% can be due to metallic impurities. The critical metals are expected to be: a) transition metals with low or mid-gap d-states, including Ti, Sc, Nd, V, Ta, Nb, b) transition metals having more d electrons than the high-κ metal, c) Cu, Ag, Ag, and d) radioactive isotopes of high-κ metals.

Table 69b Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term Years

Grey cells indicate the requirements projected only for intermediate, or long-term years. Near-term line items are not included.

Year of Production	2014	2015	2016	2017	2018	2019	2020	Driver
DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14	DRAM
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14	MPU
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6	MPU
Bulk/FDSOI/DG – Long channel electron mobility enhancement factor for MPU/ASIC [E]	1.8	1.8	1.8	1.8	1.8	1.8	1.8	MPU/ASIC
Equivalent physical oxide thickness for FDSOI MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]	0.5	0.5						MPU/ASIC
								FDSOI
Gate dielectric leakage at 100°C (A/cm^2) FDSOI high-performance [B, B1, B2]	3.30E+03	3.70E+03						MPU/ASIC
								FDSOI
Metal gate work function for FDSOI MPU/ASIC | $\phi_m - E_i$| (eV)| NMOS/PMOS [S]	+/- 0.15	+/- 0.15						MPU/ASIC
								FDSOI
Saturation velocity enhancement factor MPU/ASIC [T]	1*	1*	1*	1*	1*	1*	1*	MPU/ASIC
Si thickness FDSOI (nm) [U]	3.3	3						MPU/ASIC
								FDSOI
Maximum allowable parasitic series resistance for FDSOI NMOS MPU/ASIC × width ((Ω–μm) [G]	75	75						MPU/ASIC
								FDSOI
Maximum drain extension sheet resistance for FDSOI MPU/ASIC (NMOS) (Ω/sq) [G]	700	771						MPU/ASIC
								FDSOI
Spacer thickness, FDSOI elevated contact [J]	6.1	5.5						MPU/ASIC
								FDSOI
Thickness of FDSOI elevated junction (nm) [V}	11	10						MPU/ASIC
								FDSOI
Maximum silicon consumption for FDSOI MPU/ASIC (nm) [K]	11	10						MPU/ASIC
								FDSOI
Silicide thickness for FDSOI MPU/ASIC (nm) [L]	13	12						MPU/ASIC
								FDSOI
Contact silicide sheet R_s for FDSOI MPU/ASIC (Ω/sq) [M]	12.1	13.3						MPU/ASIC
								FDSOI
Contact maximum resistivity for FDSOI MPU/ASIC (Ω-cm^2) [N]	2.00E-08	2.00E-08						MPU/ASIC
								FDSOI
Trench fill aspect ratio – FDSOI [W]	0.6	0.6						FDSOI
Equivalent physical oxide thickness for multi-gate MPU/ASIC T_{ox} (nm) for metal gate [A, A1, A2]	0.6	0.6	0.5	0.5	0.5	0.5	0.5	MPU/ASIC
								Multigate
Gate dielectric leakage at 100°C (nA/μm) muti-gate High-performance [B, B1, B2]	1.00E+03	1.10E+03	1.20E+03	1.40E+03	1.60E+03	1.80E+03	2.20E+03	MPU/ASIC
								Multigate
Metal gate work function for multi-gate MPU/ASIC [S]	midgap	midgap	midgap	midgap	midgap	midgap	midgap	MPU/ASIC
								Multigate
Si thickness for multi-gate (nm) [U]	6.8	6.1	5.5	4.8	4.1	3.3	2.6	Multigate
Maximum allowable parasitic series resistance for multi-gate NMOS MPU/ASIC × width ((Ω–μm) [G]	85	70	65	65	60	55	50	MPU/ASIC
								Multigate
Maximum drain extension sheet resistance for multi-gate MPU/ASIC (NMOS) (Ω/sq) [G]	641	577	591	687	720	809	781	MPU/ASIC
								Multigate

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*DRAM*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*MPU*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*MPU*
Spacer thickness, multi-gate elevated contact [J]	**6.1**	**5.5**	**5**	**4.4**	**3.9**	**3.3**	**3.3**	*MPU/ASIC*
								Multigate
Thickness of multi-gate elevated junction (nm) [V]	**11**	**10**	**9**	**8**	**7**	**6**	**6**	*MPU/ASIC*
								Multigate
Maximum silicon consumption for multi-gate mpu/asic (nm) [K]	**11**	**10**	**9**	**8**	**7**	**6**	**6**	*MPU/ASIC*
								Multigate
Silicide thickness for multi-gate MPU/ASIC (nm) [L]	**13**	**12**	**11**	**10**	**8**	**7**	**7**	*MPU/ASIC*
								Multigate
Contact silicide sheet R_s for multi-gate MPU/ASIC (Ω/sq) [M]	**12.1**	**13.3**	**14.8**	**16.7**	**19**	**22.2**	**22.2**	*MPU/ASIC*
								Multigate
Contact maximum resistivity for multi-gate MPU/ASIC ($Ω$-cm^2) [N]	**2.40E-08**	**1.80E-08**	**1.50E-08**	**1.eE-08**	**1.10E-08**	**8.80E-09**	**7.00E-09**	*MPU/ASIC*
								Multigate
Physical gate length low operating power (LOP) (nm)	**14**	**13**	**11**	**10**	**9**	**8**	**7**	*LOP*
Equivalent physical oxide thickness for FDSOI low operating power T_{ox} (nm) for metal gate [A, A1, A2]	**0.8**	**0.8**	**0.7**					*LOP*
								FDSOI
Gate dielectric leakage at 100 °C for FDSOI (A/cm^2) LOP [B, B1, B2]	**3.60E+02**	**3.80E+02**	**1.10E+03**					*LOP*
								FDSOI
Metal gate work function for FDSOI and multi-gate LOP [S]	**midgap**	**midgap**	**midgap**	**midgap**	**midgap**	**midgap**	**midgap**	*LOP*
Equivalent physical oxide thickness for multi-gate low operating power T_{ox} (nm) for metal gate	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.7**	**0.7**	*LOP*
[A, A1, A2]								*Multigate*
Gate dielectric leakage at 100°C for multi-gate (A/cm^2) LOP [B, B1, B2]	**3.60E+02**	**3.80E+02**	**9.10E+02**	**1.00E+03**	**1.10E+03**	**1.30E+03**	**1.40E+03**	*LOP*
								Multigate
Physical gate length low standby power (LSTP) (nm)	**18**	**16**	**14**	**13**	**11**	**10**	**9**	*LSTP*
Equivalent physical oxide thickness for FDSOI low standby power T_{ox} (nm) for metal gate [A, A1, A2]	**1.1**	**1.1**	**1.1**	**1**	**1**	**0.9**	**0.9**	*LSTP*
								FDSOI
Gate dielectric leakage at 100°C for FDSOI (A/cm^2) LSTP [B, B1, B2]	**5.60E-02**	**6.30E-02**	**7.10E-02**	**7.70E-02**	**8.30E-02**	**9.10E-02**	**1.00E-01**	*LSTP*
								FDSOI
Metal gate work function for FDSOI and multi-gate LSTP $\lvert \phi_m - E_i \rvert$ (eV)| NMOS/PMOS [S]	**± 0.1**	**± 0.1**	**± 0.1**	**± 0.1**	**± 0.1**	**± 0.1**	**± 0.1**	*LSTP*
Equivalent physical oxide thickness for multi-gate low standby power T_{ox} (nm) for metal gate	**1**	**0.9**	**0.8**	**0.8**	**0.8**	**0.8**	**0.8**	*LSTP*
[A, A1, A2]								*Multi-gate*
Gate dielectric leakage at 100°C for multi-gate (A/cm^2) LSTP [B, B1, B2]	**6.00E-02**	**6.50E-02**	**7.50E-02**	**8.00E-02**	**8.60E-02**	**1.00E-01**	**1.30E-01**	*LSTP*
								Multi-gate
Thickness control EOT (% 3σ) [X]	**<±4**	**<±4**	**<±4**	**<±4**	**<±4**	**<±4**	**<±4**	*MPU/ASIC*
Poly-Si or Metal Gate electrode thickness (approximate) (nm) [Y]	**22**	**20**	**18**	**16**	**14**	**12**	**12**	*MPU/ASIC*
Gate etch bias (nm) [Z]	**8**	**7**	**6**	**5**	**5**	**5**	**3**	*MPU/ASIC*
L_{gate} 3σ variation (nm) [AA]	**1.32**	**1.2**	**1.08**	**0.96**	**0.84**	**0.72**	**0.72**	
Total maximum allowable lithography 3σ (nm) [AB]	**1.14**	**1.04**	**0.94**	**0.83**	**0.73**	**0.62**	**0.62**	*MPU/ASIC*

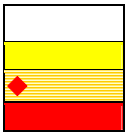
Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*DRAM*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*MPU*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	*MPU*
Total maximum allowable etch 3σ (nm), including photoresist trim and gate etch [AB]	**0.66**	**0.6**	**0.54**	**0.48**	**0.42**	**0.36**	**0.36**	*MPU/ASIC*
Resist trim maximum allowable 3σ (nm) [AC]	**0.38**	**0.35**	**0.31**	**0.28**	**0.24**	**0.21**	**0.21**	*MPU/ASIC*
Gate etch maximum allowable 3σ (nm) [AC]	**0.54**	**0.49**	**0.44**	**0.39**	**0.34**	**0.29**	**0.29**	*MPU/ASIC*
CD bias between dense and isolated lines [AD]	**≤15%**	**≤15%**	**≤15%**	**≤15%**	**≤15%**	**≤15%**	**≤15%**	*MPU/ASIC*
Minimum measurable gate dielectric remaining (post gate etch clean) [AE]	**>0**	**>0**	**>0**	**>0**	**>0**	**>0**	**>0**	*MPU/ASIC*
Profile control (side wall angle) [AF]	**90**	**90**	**90**	**90**	**90**	**90**	**90**	*MPU/ASIC*
Allowable V_t shift from charge in dielectric (mV) [AG]	**10**	**10**	**10**	**10**	**10**	**10**	**10**	*MPU/ASIC*
Allowable interfacial charge in high-κ gate stack (cm^{-2})[AH]	**2.00E+11**	**2.00E+11**	**2.00E+11**	**2.20E+11**	**2.20E+11**	**2.40E+11**	**2.40E+11**	*MPU/ASIC*
Allowable bulk charge in high-κ gate stack (cm^{-3}) [AI]	**8.90E+17**	**8.90E+17**	**8.90E+17**	**1.10E+18**	**1.10E+18**	**1.30E+18**	**1.30E+18**	*MPU/ASIC*
Allowable bulk charge in high-κ gate stack (ppm) [AI]	**40.5**	**40.5**	**40.5**	**49**	**49**	**60.5**	**60.5**	*MPU/ASIC*
Allowable critical metal impurity level in high-κ dielectric (ppm) [AJ]	**4.1**	**4.1**	**4.1**	**4.9**	**4.9**	**6.1**	**6.1**	*MPU/ASIC*

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



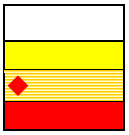
DRAM STACKED CAPACITOR

Table 70a DRAM Stacked Capacitor Films Technology Requirements—Near-term Years

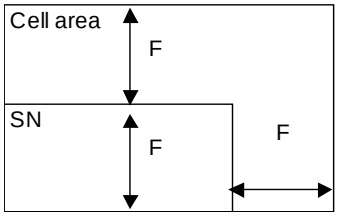
Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) [A]	80	70	65	57	50	45	40	36	32
Cell size factor a [B]	8	8	8	6	6	6	6	6	6
Cell size (μm^2) [C]	0.051 =0.16x0.32	0.041 =0.14x0.29	0.032 =0.13x0.25	0.019 =0.11x0.17	0.015 =0.10x0.15	0.012 =0.090x0.14	0.00096 =0.080x0.12	0.0077 =0.071x0.11	0.0061 =0.064x0.96
Storage node size (μm^2) [D]	0.019 =0.08x0.24	0.015 =0.071x0.21	0.012 =0.064x0.19	0.0064 =0.057x0.11	0.0051 =0.051x0.10	0.0041 =0.045x0.090	0.0032 =0.040x0.080	0.0026 =0.036x0.071	0.0020 =0.032x0.064
Capacitor structure	Cylinder /Pedestal MIM	Cylinder /Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM
t_{eq} at 25fF (nm) [G]	1.8	1.4	1.1	0.90	0.80	0.60	0.60	0.50	0.50
Dielectric constant	40	50	50	50	50	50	60	60	60
SN height (μm)	1.4	1.4	1.2	1.6	1.8	1.9	2	2	2
Cylinder factor [E]	1.5	1.5	1	1	1	1	1	1	1
Roughness factor	1	1	1	1	1	1	1	1	1
Total capacitor area (μm^2)	1.38	1.22	0.62	0.55	0.55	0.52	0.48	0.43	0.38
Structural coefficient [F]	26.8	30.0	19.2	28.6	36.0	42.6	50.2	56.3	63.2
$t_{phy.}$ at 25fF (nm) [H]	18.2	17.9	14.1	11.5	10.3	7.7	9.2	7.7	7.7
A/R of SN (OUT) for cell plate deposition [I]	32.0	39.4	33.9	47.6	60.0	64.2	92.5	98.4	121.7
HAC diameter (μm) [J]	0.10	0.09	0.08	0.07	0.06	0.05	0.05	0.04	0.04
Total interlevel insulator and metal thickness except SN (μm) [K]	0.84	0.81	0.78	0.75	0.73	0.7	0.68	0.66	0.63
HAC depth (μm) [L]	2.24	2.16	1.98	2.35	2.53	2.6	2.68	2.66	2.63
HAC A/R	23.3	25.2	25.9	34.5	41.7	48.1	55.7	62.1	68.9
$V_{capacitor}$ (Volts)	1.6	1.5	1.4	1.3	1.2	1.1	1	1	0.9
Retention time (ms) [M]	64	64	64	64	64	64	64	64	64
Leak current (fA/cell) [N]	0.94	0.88	0.82	0.76	0.70	0.64	0.59	0.59	0.53
Leak current density (nA/cm^2)	68.1	71.9	131.7	138.3	127.7	124.7	121.0	135.9	137.4
Deposition temperature (degree C)	~500	~500	~500	~500	~500	~500	~500	~500	~500
Film anneal temperature (degree C)	~750	~750	~750	~750	<750	<750	~650	~650	~650
Word line R_s (Ohm/sq.)	2	2	2	2	2	2	2	2	2

HAC—high aspect contact

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 70a and b:
[A] 2005 Overall Roadmap Technology Characteristics, Table 1a and b
[B] a = (cell size)/F^2 (F : minimum feature size)
[C] Cell size = aF^2 (cell shorter side = 2F)*
[D] SN size = (a/2 -1)F^2 (SN shorter side = F)*
[E] Cylinder structure increase the capacitor area by a factor of 1.5
[F] SC = (total capacitor area) / (cell size)
*[G] t_{eq} = 3.9*E0*(total capacitor area)/25fF*



Notes[C] & [D] Cell area and Projected SN area

[H] $t_{phy.} = t_{eq}*E_r/3.9$ If polysilicon is used as a bottom electrode. $t_{phy.} = (t_{eq}-1)*E_r/3.9$

[I] A/R of SN (OUT) = (SN height) / (F - 2 $t_{phy.}$)*

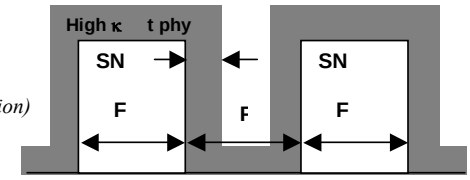
*[J] HAC diameter = 1.2*F*

[K] The thickness is assumed to be 1.05 µm@180 nm. (10% reduction by each technology generation)

[L] HAC depth = SN height + total interlevel insulator and metal thickness

[M] DRAM retention time (PIDS)

*[N] (Sense Limit*C*V_{dd}/2)/(Retention Time * MARGIN) (Sense limit=30% leak, MARGIN=100)*



Note [I] A/R of SN (OUT)

Table 70b DRAM Stacked Capacitor Films Technology Requirements—Long-term Years

Year of Production	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) [A]	28	25	22	20	18	16	14
Cell size factor a [B]	6	6	6	6	6	6	6
Cell size (μm^2) [C]	0.0048 =0.057x0.085	0.0038 =0.051x0.076	0.0030 =0.045x0.068	0.0024 =0.040x0.060	0.0019 =0.036x0.054	0.0015 =0.032x0.048	0.012 =0.028x0.043
Storage node size (μm^2) [D]	0.0016 =0.032x0.064	0.0013 =0.025x0.051	0.0010 =0.023x0.045	0.00080 =0.020x0.040	0.00064 =0.018x0.036	0.00051 =0.016x0.032	0.00040 =0.014x0.028
Capacitor structure	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM
t_{eq} at 25fF (nm) [G]	0.45	0.40	0.40	0.30	0.25	0.20	0.15
Dielectric constant	80	80	80	100	100	100	100
SN height (µm)	2	2	2	2	2	2	2
Cylinder factor [E]	1	1	1	1	1	1	1
Roughness factor	1	1	1	1	1	1	1
Total capacitor area (μm^2)	0.34	0.30	0.27	0.24	0.21	0.19	0.17
Structural coefficient [F]	70.9	79.5	89.2	100	112	126	141
t_{phy} .at 25fF (nm) [H]	9.2	8.2	8.2	7.7	6.4	5.1	3.8
A/R of SN (OUT) for cell plate deposition [I]	202.3	226.1	328.4	429.1	397.0	353.8	308.6
HAC diameter (µm) [J]	0.03	0.03	0.03	0.02	0.02	0.02	0.02
Total interlevel insulator and metal thickness except SN (µm) [K]	0.61	0.59	0.57	0.55	0.53	0.51	0.49
HAC depth (µm) [L]	2.61	2.59	2.57	2.55	2.53	2.51	2.49
HAC A/R	76.7	85.5	95.2	106.0	118.1	131.4	146.3
$V_{capacitor}$ (Volts)	0.8	0.8	0.7	0.6	0.6	0.6	0.6
Retention time (ms) [M]	64	64	64	64	64	64	64
Leak current (fA/cell) [N]	0.47	0.47	0.41	0.35	0.35	0.35	0.35
Leak current density (nA/cm^2)	137.1	154.0	151.3	145.7	163.6	183.7	206.2
Deposition temperature (degree C)	~500	~500	~500	~500	~500	~500	~500
Film anneal temperature (degree C)	<650	<650	<650	<650	<650	<650	<650
Word line R_s (Ohm/sq.)	2	2	2	2	2	2	2

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

WAS

	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
DRAM M1 ½ -pitch (nm)			65			45			32			22			16	
Top Electrode	Metal: Ti, TiN, W, Pt, Ru, RuO_2, IrO_2, ...															
Capacitor Dielectric Material	Al_2O_3, HfO_2, Ta_2O_5			Ta_2O_5, TiO_2			Ultra high κ; new materials, strontium -based, perovskites									
Bottom Electrode	Metal: Ti, TiN, W, Pt, Ru, RuO_2, IrO_2, others															

IS

	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
DRAM M1 ½ -pitch (nm)			65			45			32			22			16	
Top Electrode	Metal: Ti, TiN, W, Pt, Ru, RuO_2, IrO_2, ...															
Capacitor Dielectric Material	Al_2O_3 Ta_2O_5	Al_2O_3 , HfO_2 Ta_2O_5, TiO_2, ZrO_2					Ultra high κ; new materials, strontium -based, perovskites									
Bottom Electrode	Metal: Ti, TiN, W, Pt, Ru, RuO_2, IrO_2, others															

Figure 61 DRAM Stacked Capacitor Potential Solutions UPDATED [19]

DRAM TRENCH CAPACITOR

Table 71a DRAM Trench Capacitor Technology Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	Cell size factor	8	8	8	8	8	8	8	8	8
	Cell size (μm^2)	0.051	0.039	0.034	0.026	0.020	0.016	0.013	0.010	0.008
	Trench structure	bottled	bottled	bottled	bottled	bottled	bottled	bottled	bottled	bottled
	Trench circumference (nm)	665	582	540	474	416	374	333	291	266
	Trench area enhancement factor (bottle) [A]	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6	1.6
	Trench surface roughening factor	1.25	1.25	1.2	1	1	1	1	1	1
WAS	Effective oxide thickness (CET)(nm)	4.4	4.3	3.9	2.8	2.3	2.0	1.8	1.6	1.4
IS	Effective oxide thickness (CET)(nm)	4.4	4.3	3.9	2.8	2.3	1.8	1.4	1.1	0.9
	Trench depth [µm], (at 35fF)	6.2	6.8	6.8	6.7	6.2	6.1	6.2	6.1	6.0
WAS	Aspect ratio (trench depth/trench width)	60	75	80	90	95	105	120	135	145
IS	Aspect ratio (trench depth/trench width)	60	75	80	90	95	95	95	95	95
	Upper electrode	Poly-Silicon	Poly-Silicon	Metal	Metal	Metal	Metal	Metal	Metal	Metal
WAS	Dielectric material	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ
IS	Dielectric material	NO	NO	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ
	Bottom electrode	Silicon	Silicon	Silicon	Silicon	Silicon	1: Silicon	1: Silicon	Metal	Metal
						2: Metal	2: Metal	2: Metal		
	Capacitor structure/dielectric	Silicon-Insulator-Silicon/High-κ		Meal-Insulator-Silicon/High-κ		1: MIS/High-κ 2: MIM/High-κ			Metal-Insulator-Metal / High-κ	

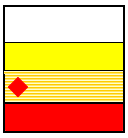
[A] Bottle factor = checkerboard square perimeter / conventional elliptical perimeter
Perimeter of trench ellipse = pi(3/2(a+b)-sqrt(ab))= 7,933 * short half axis*

Table 71b DRAM Trench Capacitor Technology Requirements—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	Cell size factor	8	8	8	8	8	8	8
	Cell size (μm^2)	0.006	0.005	0.004	0.003	0.003	0.002	0.002
	Trench structure	bottled	bottled	bottled	bottled	bottled	bottled	bottled
	Trench circumference (nm)	233	208	183	166	150	133	116
	Trench area enhancement factor (bottle) [A]	1.6	1.6	1.6	1.6	1.6	1.6	1.6
	Trench surface roughening factor	1	1	1	1	1	1	1
WAS	Effective oxide thickness (CET)(nm)	1.2	1.0	0.8	0.7	0.6	0.5	0.4
IS	Effective oxide thickness (CET)(nm)	0.7	0.7	0.6	0.6	0.5	0.4	0.4
WAS	Trench depth [µm], (at 35fF)	5.8	5.5	5.0	4.8	4.5	4.2	3.8
IS	Trench depth [µm], (at 35fF)	3.6	3.9	5.0	4.8	4.5	4.2	3.8
WAS	Aspect ratio (trench depth/trench width)	160	170	175	185	190	200	210
IS	Aspect ratio (trench depth/trench width)	100	120	140	154	160	183	210
	Upper electrode	Metal	Metal	Metal	Metal	Metal	Metal	Metal
	Dielectric material	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ	High-κ
	Bottom electrode	Metal	Metal	Metal	Metal	Metal	Metal	Metal
	Capacitor structure/dielectric	Metal-Insulator-Metal/High-κ						

[A] Bottle factor = checkerboard square perimeter / conventional elliptical perimeter
Perimeter of trench ellipse = pi(3/2(a+b)-sqrt(ab)) = 7,933 * short half axis*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



NON-VOLATILE MEMORY (FLASH)

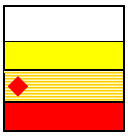
Table 72a FLASH Non-volatile Memory Technology Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	Flash technology generation NOR/NAND - F (nm) [A]	80/70	70/65	65/55	57/50	50/45	45/40	40/35	35/32	32/28
	Flash NOR tunnel oxide thickness (EOT-nm) [B]	8–9	8–9	8–9	8–9	8–9	8	8	8	8
	Flash NAND tunnel oxide thickness (EOT-nm) [B]	7–8	7–8	6–7	6–7	6–7	6–7	6–7	6–7	6–7
	Flash program/erase window min DVT SLC/MLC (V) [D]	1.5/2.4	1.5/2.4	1.5/2.4	1.5/2.4	1.5/2.4	1.5/2.4	1.5/2.4	1.5/2.4	1.5/2.4
	Flash erase/program time degradation t_{max}/t_0 at constant V [E]	<2	<2	<2	<2	<2	<2	<2	<2	<2
	Flash NOR interpoly dielectric thickness (EOT-nm) [F]	13–15	13–15	13–15	13–15	13–15	◆ 6–13	◆ 6–13	◆ 6–13	4–6
	Flash NAND interpoly dielectric thickness (EOT-nm) [F]	13–15	13–15	10–13	10–13	10–13	◆ 5–12	◆ 5–12	◆ 5–12	4–6
	Flash interpoly dielectric thickness control EOT (% 3s) [G]	<±6	<±6	<±6	<±6	<±6	<±5	<±5	<±5	<±5
	Flash interpoly dielectric T_{max} of formation t >5'/<5' (ºC) [H]	750/900	750/900	750/900	750/900	750/900	650/800	650/800	650/800	600/700
	Flash interpoly dielectric conformality on floating gate EOT_{min}/EOT_{max} [I]	>0.98	>0.98	>0.98	>0.98	>0.98	>0.98	>0.98	>0.98	>0.98
	Tunnel / Interpoly max leakage current (A) at 2 V for 10 years data retention [J]	1 E-24	1 E-24	5 E-25	5 E-25	5 E-25	2.5E-25	2.5E-25	2.5E-25	1.3E-25
ADD	STI Filling Aspect Ratio(min-max) [K]		3.0- 4.7	3.2-5.3	3.5– 5.8	3.9-6.4	4.2-7.1	4.6-7.8	5.0-8.6	5.5-9.7

Table 72b FLASH Non-volatile Memory Technology Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	Flash technology generation NOR/NAND - F (nm) [A]	**28/25**	**25/22**	**22/20**	**20/18**	**18/16**	**16/14**	**14/12**
	Flash NOR tunnel oxide thickness (EOT-nm) [B]	**7–8**	**7–8**	**7–8**	**7–8**	**7–8**	**7–8**	**7–8**
	Flash NAND tunnel oxide thickness (EOT-nm) [B]	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**	**6–7**
	Flash program/erase window min DVT SLC/MLC (V) [D]	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**	**1.5/2.4**
	Flash erase/program time degradation t_{max}/t_0 at constant V [E]	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**	**<2**
	Flash NOR interpoly dielectric thickness (EOT-nm) [F]	**4–6**	**4–6**	**3–5**	**3–5**	**3–5**	**3–5**	**3–5**
	Flash NAND interpoly dielectric thickness (EOT-nm) [F]	**4–6**	**4–6**	**3–5**	**3–5**	**3–5**	**3–5**	**3–5**
	Flash interpoly dielectric thickness control EOT (% 3s) [G]	**<±5**	**<±5**	**<±5**	**<±5**	**<±5**	**<±5**	**<±5**
	Flash interpoly dielectric T_{max} of formation t >5'/<5' (ºC) [H]	**600/700**	**600/700**	**600/700**	**600/700**	**600/700**	**600/700**	**600/700**
	Flash interpoly dielectric conformality on floating gate EOT_{min}/EOT_{max} [I]	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**	**>0.98**
	Tunnel / Interpoly max leakage current (A) at 2 V for 10 years data retention [J]	**1.3E-25**	**1.3E-25**	**6E-26**	**6E-26**	**6E-26**	**3E-26**	**3E-26**
ADD	*STI Filling Aspect Ratio(min-max) [K]*	**>6-10**	**>6-10**	**>6-10**	**>6-10**	**>6-10**	**>6-10**	**>6-10.**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 72a and b:
[A] In the past Flash devices tended to lag behind the current CMOS technology generation, but that delay no longer exists. This entry provides the F value for designs in the indicated time period.
[B] Tunnel oxides must be thick enough to assure retention but thin enough to allow ease of erase/write. This difficult trade off problem hinders scaling. Tunnel oxides less than 7 nm seem to pose fundamental problems for retention reliability.
[C] Tunnel oxide thickness control must guarantee correct program/erase window
[D] Between minimum and maximum values of the program/erase distributions for Single/Multilevel cells (SLC/MLC)
[E] Time degradation after maximum specification number of write/erase cycles considering no erasing/program voltage correction
F] Interpoly dielectric must be thick enough to assure retention but thin enough to assure an almost constant coupling ratio. Charge retention when the dielectric is scaled downward is the major issue. High-κ interpoly will help reducing the interpoly EOT and maintain constant coupling ratio without loosing retention.
[G] Thickness control to assure correct coupling ratio and minimum thickness for charge retention
[H] For long (>5 min) and short (<5 min) thermal processes to avoid tunnel oxide and device degradation
[I] Uniform step coverage is important to assure charge retention, especially when the floating gate sidewall is electrically coupled with the control gate to enhance the coupling ratio
[J] Maximum leakage current through the tunnel and interpoly dielectrics to assure 10 years data retention. It is calculated considering a floating gate voltage of -2 V when the cell is programmed and a total capacitance that is a half every technology generation. In case of 20 years data retention the leakage current target value is 50% than the reported value.

ADD	***[K] Ratio between the height and the length of the trench to be filled .Minimum value is typically for NOR without drain silicidation, maximum value is typically for NAND. Height of the trench includes both the height of the stack outside silicon and the depth of the silicon trench. Actual considered vertical dimensions are based on literature data and the future trend is based on some overall reduction for NOR, due to operating voltage scaling, and no silicon trench reduction for NAND, due to hard scaling of the operating voltage. Length of the trench is the minimum feature size given for the technology generation, or higher.[20,21]***

PHASE CHANGE MEMORY

Table PCM Phase Change Memory (PCM) Technology Requirements—Near-term Years

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
Phase Change Technology Generation (nm)	-	70	65	57	50	45	40	35	32
PCRAM phase change material conformality (%) [A]	-	>30	>30	>60	>60	>60	>90	>90	>90
PCRAM phase change material minimum operating temperature (°C) [B]	-	85	85	100	100	100	125	125	125

[A] Conformality requirements of the phase change material are given for μ–trench PCRAM to optimize the operating current and the formation technology [22,23,24,25]

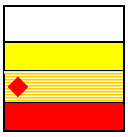
[B] Minimum operating temperature for all PCRAM architectures to guarantee >10 years data retention as per PIDS table 43a and 43b

FERROELECTRIC RANDOM ACCESS MEMORY (FERAM)

Table 73a FeRAM Technology Requirements—Near-term Years

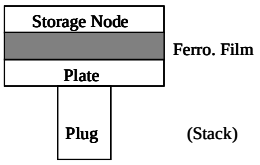
Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
Feature size (μm) [A]	0.13	0.11	0.10	0.09	0.08	0.065	0.057	0.05	0.045
Access time (ns) [B]	30	30	20	20	20	15	15	15	10
Cycle time (ns) [C]	50	50	30	30	30	25	25	25	16
Cell area factor: a [D]	34	34	30	30	30	24	24	24	20
Cell size (μm^2) [E]	0.575	0.411	0.300	0.243	0.192	0.101	0.078	0.060	0.041
Capacitor footprint (μm^2) [F]	0.32	0.23	0.158	0.128	0.101	0.049	0.038	0.029	0.018
Capacitor active area (μm^2) [G]	0.32	0.23	0.158	0.128	0.101	0.076	0.069	0.064	0.059
Cap active area/footprint ratio [H]	1.00	1.00	1.00	1.00	1.00	1.55	1.85	2.20	3.31
Height of bottom electrode/F (for 3D capacitor) [I]	n/a	n/a	n/a	n/a	n/a	0.80	1.23	1.73	2.55
Capacitor structure [J]	stack	stack	stack	stack	stack	3D	3D	3D	3D
Cell structure [K]	1T1C	1T1C	1T1C	1T1C		1T1C	1T1C	1T1C	1T1C
V_{op} (Volt) [L]	1.5	1.5	1.2	1.2	1.2	1.0	1.0	1.0	0.7
Minimum switching charge density ($\mu C/cm^2$) at V_{op} [M]	11.4	14.2	19	22	26	30	30	30	30
Minimum switching charge per cell (fC/cell) at V_{op} [N]	36.1	32.3	30.3	28.2	26.1	22.7	20.8	19.1	17.8
Retention at 85°C (Years) [O]	10	10	10	10	10	10	10	10	10
Endurance [P]	1.0E+13	1.0E+14	1.0E+15	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 73a and b:
[A] Feature size "F" is defined as the critical dimension in the cell from the first two companies in mass production, regardless of whether the FeRAM is stand-alone or embedded.
[B] Not referenced.
[C] Not referenced.

[D] a = Cell size/$F1^2$.
[E] Cell size = a $F1^2$.*
[F] {(cell size)$^{1/2}$ – (capacitor space)}^{2} is assumed, where capacitor space = 1.5 F.*
[G] 3D is assumed to be a pedestal structure.
[H] More than 1 for 3D capacitors, otherwise: 1.
*[I] For instance, 0.24 means that the height is 0.24*F.*
[J] See figures (right).
[K] Besides cell structures, configurations are being investigated; ex. Chain-FeRAM.
[L] V_{op}=operational voltage. Low voltage operation is a key issue. Matsushita's 0.18 μm sample with SBT at 2003: 1.1V.
[M] This value can be calculated by [S] divided by [L]. This value is assumed to be 40 for 3D.
*[N] Calculated by $\Delta V_{bitline}$*$C_{bitline}$ with the assumptions that $\Delta V_{bitline}$=140 mV is needed and $C_{bitline}$ is as same as DRAM.*
[O] Depends on applications. 85°C comes from the specifications for IC cards.
*[P] 100 MHz*10 years=3E+16. Some 1E+15 is required to compete with SRAM and DRAM.*



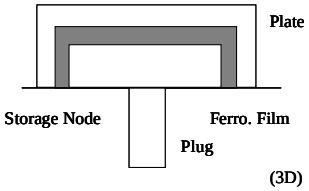


Table 73b FeRAM Technology Requirements—Long-term Years

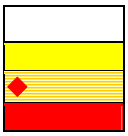
Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
Feature Size (μm) [A]	0.04	0.035	0.032	0.028	0.025	0.022	0.02
Access time (ns) [B]	10	10	8	8	8	6	6
Cycle time (ns) [C]	16	16	12	12	12	10	10
Cell area factor: a [D]	20	20	16	16	16	14	14
Cell size (μm^2) [E]	0.032	0.025	0.016	0.013	0.010	0.007	0.006
Capacitor footprint (μm^2) [F]	0.014	0.011	0.0064	0.0049	0.0039	0.0024	0.0020
Capacitor active area (μm^2) [G]	0.055	0.050	0.047	0.043	0.040	0.037	0.035
Cap active area/footprint ratio [H]	3.88	4.63	7.38	8.81	10.25	15.12	17.17
Height of bottom electrode/F (for 3D capacitor) [I]	3.18	4.01	4.98	6.11	7.23	8.87	10.16
Capacitor structure [J]	3D	3D	3D	3D	3D	3D	3D
Cell structure [K]	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C
V_{op} (Volt) [L]	0.7	0.7	0.7	0.7	0.7		
Minimum switching charge density (uC/cm^2) at V_{op} [M]	30	30	30	30	30	30	30
Minimum switching charge per cell (fC/cell) at V_{op} [N]	16.4	15.0	14.2	13.0	12.0	11.0	10.4
Retention at 85°C (Years) [O]	10	10	10	10	10	10	10
Endurance [P]	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16	>1.0E16

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known



ADD

Although BFO exhibits a large polarization, it also requires a higher switching voltage which means that the film needs to be thinner or possibly doped to accommodate low voltage operation. Since the ferroelectric properties of each material have improved in recent years, it essential to master the material processing conditions for the ferroelectric material.

WAS

Year of First Product Shipment	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Ferroelectric Materials	PZT, SBT							PZT, SBT, New Materials								
Deposition Methods	PVD, CSD, MOCVD				MOCVD, New Methods											

CSD – Chemical Solution Deposition

PZT – P $(Zr, Ti)O_3$

SBT – $SrBi_2Ta_2O_9$

*Figure 65 FeRAM Potential Solutions **WAS***

IS

Year of First Product Shipment	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Ferroelectric Materials	PZT, SBT							PZT, SBT, New Materials (BFO)								
Deposition Methods	PVD, CSD, MOCVD				MOCVD, New Methods											

CSD – Chemical Solution Deposition

PZT – Pb $(Zr, Ti)O_3$

SBT – $SrBi_2Ta_2O_9$

BFO – $BiFeO_3$

*Figure 65 FeRAM Potential Solutions **IS***

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