INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2006 UPDATE

OVERVIEW AND WORKING GROUP SUMMARIES

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OVERVIEW

The International Technology Roadmap for Semiconductors (ITRS) is the result of a worldwide consensus-building process. This document predicts the main trends in the semiconductor industry spanning across 15 years into the future. The participation of experts from Europe, Japan, Korea, and Taiwan as well as the U.S.A. ensures that the ITRS is a valid source of guidance for the semiconductor industry as we strive to extend the historical advancement of semiconductor technology and the worldwide integrated circuit (IC) market. These five regions jointly sponsor the ITRS.

The Semiconductor Industry Association (SIA) coordinated the first efforts of producing what was originally *The National Technology Roadmap for Semiconductors* (*NTRS*). The semiconductor industry became a global industry in the 1990s, as many semiconductor chip manufacturers established manufacturing or assembly facilities in multiple regions of the world. This realization led to the creation of the *International Technology Roadmap for Semiconductors* in the late 90s. The invitation to cooperate on the ITRS was extended by the SIA at the World Semiconductor Council in April 1998 to Europe, Japan, Korea, and Taiwan. Since then, full revisions of the ITRS were produced in 1999, 2001, 2003 and 2005; ITRS updates were produced in the even-numbered years (2000, 2002, and 2004).

The ITRS process is an ongoing event. The industry is dynamic—continually innovating; introducing new products; and achieving solutions. To keep the ITRS information as current as possible with this dynamic industry environment, during each year following an edition such as the *2005 ITRS,* the roadmap information is reviewed. Data adjustments, corrections, and new information items are agreed to among the ITWG members and by soliciting public feedback during the annual ITRS Summer Conference in San Francisco. For the *2006 ITRS Update* effort, all the ITRS tables were reviewed. If necessary, data and notations were updated to match industry advancements.

Overall, the *2006 ITRS Update* represents a minor modification to the *2005 ITRS*. The *2006 ITRS Update*, consistent with the *2005 ITRS*, removes the concept of "technology node" as the main pace setter for the IC industry. Users of the 2006 Update easily can determine specific numbers for DRAM metal half-pitch, NAND polysilicon half-pitch, or MPU and ASIC gate length, for example, to characterize the pace of that specific technology. The Overall Roadmap Technology Characteristics Tables and individual ITWG tables use these specific product timings to indicate the drivers for their requirements. For this purpose, the *2006 ITRS Update* addresses an independent measure of the technology pace of DRAM, of MPU, and of Flash products.

Several tables have been corrected or updated, as clearly indicated in blue. It is also rather easy to identify where the changes have occurred as indicated by "**IS"** in the far left column of an updated table. This Overview document contains an Appendix of all tables, figures, or textual changes for the *2006 Update* by chapter.

It is important to remind the reader that it is the purpose of the ITRS documents to provide a reference of requirements, potential solutions, and their timing for the semiconductor industry. This objective has been accomplished by providing a forum for international discussion, cooperation, and agreement among the leading semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university, consortia, and government labs.

The ITRS documents have become and remain a truly common reference for the entire semiconductor industry. Indeed, the cooperative efforts of the ITRS participants have fostered cooperation among international consortia, universities, and research institutions around the world. It is hoped that the *2006 ITRS* Update will further contribute to fuel cooperative R&D investments so that the financial burden can be more uniformly shared by the whole industry. It is also hoped that the ITRS will continue to stimulate the fundamental elements that encourage innovation in individual companies.

OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS

SUMMARY

The International Technology Roadmap for Semiconductors (ITRS) Overall Roadmap Technology Characteristics (ORTC) section provides both originating guidance from ORTC Product Models and also consolidates items from other ITRS Technology Working Group (TWG) tables.

Table 1a-h Product Generations (DRAM, Flash, MPU/ASIC) and Chip Size Model Technology Trends—There are no changes from the 2005 ORTC Technology Trend and Product Models, and there are also no changes to the 2005 Product Performance Models provided by the Design TWG. As a result, the ORTC Tables 1a-i, which are sourced from those models, remain unchanged. There are some corrections made to the line item labels: 1) various cell area and transistor area labels, which were incorrectly labeled as "mm^2" in the 2005 tables, instead of "um^2"; and 2) Flash Memory bits per cm^2 labeled "Gbits/cm^2" (Giga-bits/ $cm^{2)}$ rather than "Bits/cm^2." The remaining changes to ORTC tables for the 2006 Update are derived from corresponding changes to TWG tables, which are used as the various source line items for consolidation in the ORTC. A review of these TWG-related ORTC Tables is included below.

Table 2a&b Lithographic-Field and Wafer-Size Trends—Lithography field size trends are unchanged. Wafer generation targets (450mm target to begin in 2012 on 11-year cycle) remain unchanged by the International Roadmap Committee (IRC). It is important to note that dialogue is underway between semiconductor manufacturers and suppliers to assess standards and productivity improvement options on 300mm and 450mm generations. Economic analysis of option scenarios is also underway to examine the required R&D cost, benefits, return-on-investment, and funding mechanism analysis and proposals.

Table 3a&b Performance of Packaged Chips: Number of Pads and Pins—Internal chip pad counts for both I/O and power and ground remain unchanged (2:1 ratio I/O-to-power/ground for high-performance MPU; 1:1 ratio for high-performance ASIC). After assessment of the progress in the back-end assembly and packaging industry, the Assembly and Packaging (A&P) TWG increased their numerical targets and trends for the maximum pin counts, increasing pressure on future packaging costs.

Table 4a&b Performance and Package Chips: Pads, Cost—The A&P TWG increased the area array flip chip pad spacing targets by 10–20%. The two-row staggered-pitch targets have increased 10–20% in the near termand the three-row staggered-pitch targets have increased 10–50% in the near term. Both pitch targets remain unchanged in the long term. Cost-per-pin targetsare adjusted by the A&P TWG, to reflect estimates and response to cost challenges.

Table 4c&d Performance and Package Chips: Frequency On-chip Wiring Levels—The A&P TWG adjusted the chip-to-board (off-chip) frequency targets in the 2011–2020 range to remain below the Design/Process Integration (PIDS) targets for on-chip frequency. The Design/PIDS targets for on-chip frequency remain unchanged in the 2006 Update. The Interconnect TWG leaves thenumber of on-chip wiring levels unchanged.

Table 5a&b Electrical Defects—The MPU and DRAM defect targets are adjusted by the Yield Enhancement TWG to reflect their new 2006 Update models and trends, in which both random defects/cm^2 and the number of mask levels have leveled off through 2020 at smaller long range targets.

Table 6a&b Power Supply and Power Dissipation—There are no changes to the PIDS TWG MPU and DRAM targets for voltage. The A&P TWG kept the maximum power per square centimeter targets unchanged through 2018. The 2019 and 2020 targets, which increased in the 2005 table, are constant in the update table. The maximum Watts (calculated by the ORTC table for specific product maximum production start chip sizes) are also now constant targets in 2019 and 2020.

Table 7a&b Cost—The "tops-down" semiconductor market driver models for cost-per-function remain unchanged for the the 2006 Update. The Cost table targets for both memory and logic represent the need to preserve the historical economic semiconductor device productivity trend for continuous reduction of the cost-per-function by -29% compound annual reduction rate (CARR) throughout the roadmap timeframe.

Preserving this cost-per-function productivity trend in view of increasing packaging costs, plus the slowing of product function densities due to slower technology cycles (three-year versus two-year) and design factor improvements, represent the over-arching economic grand challenge for the industry.

Table 1a Product Generations and Chip Size Model Technology Trend Targets—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Printed Gate Length (nm) ††	**54**	**48**	**42**	**38**	**34**	**30**	**27**	**24**	**21**
MPU Physical Gate Length (nm)	**32**	**28**	**25**	**23**	**20**	**18**	**16**	**14**	**13**
ASIC/Low Operating Power Printed Gate Length (nm) ††	**76**	**64**	**54**	**48**	**42**	**38**	**34**	**30**	**27**
ASIC/Low Operating Power Physical Gate Length (nm)	**45**	**38**	**32**	**28**	**25**	**23**	**20**	**18**	**16**
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**76**	**64**	**57**	**51**	**45**	**40**	**36**	**32**	**28**

Table 1b Product Generations and Chip Size Model Technology Trend Targets—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Printed Gate Length (nm) ††	**19**	**17**	**15**	**13**	**12**	**11**	**9**
MPU Physical Gate Length (nm)	**11**	**10**	**9**	**8**	**7**	**6**	**6**
ASIC/Low Operating Power Printed Gate Length (nm) ††	**24**	**21**	**19**	**17**	**15**	**13**	**12**
ASIC/Low Operating Power Physical Gate Length (nm)	**14**	**13**	**11**	**10**	**9**	**8**	**7**
Flash ½ Pitch (nm) (un-contacted Poly)(f)	**25**	**23**	**20**	**18**	**16**	**14**	**13**

Notes for Tables 1a and 1b:

†† MPU and ASIC gate-length (in resist) node targets refer to the most aggressive requirements, as printed in photoresist (which was by definition also "as etched in polysilicon," in the 1999 ITRS).

However, during the 2000/2001 ITRS development, trends were identified, in which the MPU and ASIC "physical" gate lengths may be reduced from the "as-printed" dimension. These physical gate-length targets are driven by the need for maximum speed performance in logic microprocessor (MPU) products, and are included in the Front End Processes (FEP), Process Integration, Devices, and Structures (PIDs), and Design chapter tables as needs that drive device design and process technology requirements.

Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

MPU Physical Gate Length targets are unchanged from the 2003 ITRS and 2004 ITRS Update, but also included are the complete set of annualized Long-term targets through 2020. The printed gate length has been adjusted to reflect the agreement between the FEP and Lithography TWGs to use a standard factor, 1.6818, to model the relationship between the final physical gate length and the printed gate length, after additional processing is applied to that isolated feature.

MPU/ASIC M1 stagger-contact targets have been accelerated to 90 nm in 2005 to reflect actual industry performance per the Interconnect ITWG recommendation, and a new consensus model technology cycle timing of 2.5 years (to 0.71× reduction) has been applied through 2010, when the trend targets become equal to the DRAM stagger-contact M1 through 2020.

Numbers in the header are rounded from the actual trend numbers used for calculation of models in ITRS ORTC and ITWG tables (see discussion in the Executive Summary on rounding practices).

Table 1c DRAM and Flash Production Product Generations and Chip Size Model—Near-term Years
UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	DRAM Product Table									
	Cell area factor [a]	8	8	8	6	6	6	6	6	6
IS	Cell area [Ca = af2] (μm²)	0.051	0.041	0.032	0.019	0.015	0.012	0.0096	0.0077	0.0061
	Cell array area at production (% of chip size) §	63.00%	63.00%	63.00%	56.08%	56.08%	56.08%	56.08%	56.08%	56.08%
	Generation at production §	1G	2G	2G	2G	4G	4G	4G	8G	8G
	Functions per chip (Gbits)	1.07	2.15	2.15	2.15	4.29	4.29	4.29	8.59	8.59
	Chip size at production (mm^2)§	88	139	110	74	117	93	74	117	93
	Gbits/cm2 at production §	1.22	1.54	1.94	2.91	3.66	4.62	5.82	7.33	9.23
	Flash Product Table									
	Flash ½ Pitch (nm) (un-contacted Poly)(f)	75.7	63.6	56.7	50.5	45.0	40.1	35.7	31.8	28.3
	Cell area factor [a]	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0	4.0
IS	Cell area [Ca = af^2] (μm²)	0.023	0.016	0.013	0.010	0.008	0.006	0.005	0.004	0.003
	Cell array area at production (% of chip size) §	67.5%	67.5%	67.5%	67.5%	67.5%	67.5%	67.5%	67.5%	67.5%
	Generation at production § SLC	4G	4G	4G	8G	8G	8G	16G	16G	16G
	Generation at production § MLC	8G	8G	8G	16G	16G	16G	32G	32G	32G
	Functions per chip (Gbits) SLC	4.29	4.29	4.29	8.59	8.59	8.59	17.18	17.18	17.18
	Functions per chip (Gbits) MLC	8.59	8.59	8.59	17.18	17.18	17.18	34.36	34.36	34.36
	Chip size at production (mm^2)§ SLC	144	101.8	80.8	128.3	101.8	80.8	128.3	101.8	80.8
	Chip size at production (mm^2)§ MLC	144	101.8	80.8	128.3	101.8	80.8	128.3	101.8	80.8
IS	Bits/cm^2 at production § SLC	3.0E+09	4.2E+09	5.3E+09	6.7E+09	8.4E+09	1.1E+10	1.3E+10	1.7E+10	2.1E+10
IS	Bits/cm^2 at production § MLC	6.0E+09	8.4E+09	1.1E+10	1.3E+10	1.7E+10	2.1E+10	2.7E+10	3.4E+10	4.3E+10

Table 1d DRAM and Flash Production Product Generations and Chip Size Model—Long-term Years
UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	DRAM Product Table							
	Cell area factor [a]	6	6	6	6	6	6	6
IS	Cell area [Ca = af^2] (μm^2)	0.0048	0.0038	0.0030	0.0024	0.0019	0.0015	0.0012
	Cell array area at production (% of chip size) §	56.08%	56.08%	56.08%	56.08%	56.08%	56.08%	56.08%
	Generation at production §	8G	16G	16G	16G	32G	32G	32G
	Functions per chip (Gbits)	8.59	17.18	17.18	17.18	34.36	34.36	34.36
	Chip size at production (mm^2)§	74	117	93	74	117	93	74
	Gbits/cm2 at production §	11.63	14.65	18.46	23.26	29.31	36.93	46.52
	Flash Product Table							
	Flash ½ Pitch (nm) (un-contacted Poly)(f)	25.3	22.5	20.0	17.9	15.9	14.2	12.6
	Cell area factor [a]	4.0	4.0	4.0	4.0	4.0	4.0	4.0
IS	Cell area [Ca = af^2] (μm^2)	0.003	0.002	0.002	0.001	0.001	0.001	0.001
	Cell array area at production (% of chip size) §	67.5%	67.5%	67.5%	67.5%	67.5%	67.5%	67.5%
	Generation at production § SLC	32G	32G	32G	64G	64G	64G	128G
	Generation at production § MLC	64G	64G	64G	128G	128G	128G	256G
	Functions per chip (Gbits) SLC	34.36	34.36	34.36	68.72	68.72	68.72	137.44
	Functions per chip (Gbits) MLC	68.72	68.72	68.72	137.44	137.44	137.44	274.88
	Chip size at production (mm^2)§ SLC	128.3	101.8	80.8	128.3	101.8	80.8	128.3
	Chip size at production (mm^2)§ MLC	128.3	101.8	80.8	128.3	101.8	80.8	128.3
IS	Bits/cm^2 at production § SLC	2.7E+10	3.4E+10	4.3E+10	5.4E+10	6.7E+10	8.5E+10	1.1E+11
IS	Bits/cm^2 at production § MLC	5.4E+10	6.7E+10	8.5E+10	1.1E+11	1.3E+11	1.7E+11	2.1E+11

Notes for Tables 1c and 1d:
§ DRAM Model—cell area factor (design/process improvement) targets are as follows:
1999–2007/8×: 2008-2020/6×. Due to the elimination of the "7.5," "7,"and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.
DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the latest model 2005 ITRS timeframe refer to Figures 9 and 10 for bit size and bits/chip trends:
1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).
As a result of the DRAM consensus model changes for the 2005 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM products remains "flat" at less than 140 mm^2, similar to the MPU model. However, with the elimination of some of some of "cell area factor" reductions, the flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c, 1d).
Furthermore, the cell array efficiency (CAE – the Array % of total chip area) was corrected to 56.1% after 2008, since only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery. This CAE change in the model puts even additional pressure on the production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.
Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.
Similarly to DRAM, the new Flash product model also targets an affordable (<145 mm^2) chip size and includes a doubling of functions (bits) per chip every technology cycle (three years after 2006) on an Inter-generation. Flash cells have reached a limit of the 4-design factor, so the reduction of the Flash single-level cell (SLC) size is paced by the uncontacted polysilicon (three-year cycle). However, the Flash technology has the ability to store and electrically access two bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half the size of an SLC product cell size (refer to Figures 9 and 10).

Table 1e DRAM Introduction Product Generations and Chip Size Model—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	Cell area factor [a]	8	8	8	6	6	6	6	6	6
IS	Cell area [Ca = af^2] (μm^2)	0.051	0.041	0.032	0.019	0.015	0.012	0.010	0.008	0.006
	Cell array area at introduction (% of chip size) §	72.95%	73.25%	73.52%	73.76%	73.97%	74.16%	74.30%	74.47%	74.61%
	Generation at introduction §	8G	8G	16G	16G	16G	32G	32G	32G	64G
	Functions per chip (Gbits)	8.59	8.59	17.18	17.18	17.18	34.36	34.36	34.36	68.72
	Chip size at introduction (mm^2) §	606	479	757	449	356	563	446	353	560
	$Gbits/cm^2$ at introduction §	1.42	1.79	2.27	3.82	4.83	6.10	7.70	9.73	12.28

Table 1f DRAM Introduction Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	Cell area factor [a]	6	6	6	6	6	6	6
IS	Cell area [Ca = af^2] (μm^2)	0.005	0.004	0.003	0.002	0.002	0.002	0.001
	Cell array area at introduction (% of chip size) §	74.70%	74.83%	74.93%	75.00%	75.09%	75.18%	75.27%
	Generation at introduction §	64G	64G	128G	128G	128G	256G	256G
	Functions per chip (Gbits)	68.72	68.72	137.44	137.44	137.44	274.88	274.88
	Chip size at introduction (mm^2) §	444	351	557	442	350	555	440
	$Gbits/cm^2$ at introduction §	15.49	19.55	24.67	31.11	39.24	49.50	62.44

Notes for Tables 1e and 1f:
§ DRAM Model—cell area factor (design/process improvement) targets are as follows:
1999–2007/8×: 2008-2020/6×. Due to the elimination of the "7.5," "7," and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.
DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the latest model 2005 ITRS timeframe:
1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and
2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).
As a result of the DRAM consensus model changes for the 2005 ITRS, the InTER-generation chip size growth rate model target for production-phase DRAM products remains "flat" at less than 140 mm^2, similar to the MPU model. However, with the elimination of some of some of "cell area factor" reductions, the flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per three years (see ORTC Table 1c, d).
Furthermore, the cell array efficiency (CAE – the Array % of total chip area) was corrected to 56.1% after 2008, since only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery. This CAE change in the model puts even additional pressure on the Production-phase product chip size to meet the target flat-chip-size model. It can be observed in the Table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.
Refer to the Glossary for definitions of Introduction, Production, InTERgeneration, and InTRAgeneration terms.

Table 1g MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	51	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	SRAM Cell (6-transistor) Area factor ++	**91.8**	**94.5**	**97.5**	**100.7**	**104.1**	**107.8**	**106.7**	**105.7**	**104.8**
	Logic Gate (4-transistor) Area factor ++	**254**	**266**	**279**	**292**	**306**	**320**	**320**	**320**	**320**
	SRAM Cell (6-transistor) Area efficiency ++	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**	**0.63**
	Logic Gate (4-transistor) Area efficiency ++	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**	**0.50**
IS	SRAM Cell (6-transistor) Area (μm^2)++	**0.74**	**0.58**	**0.45**	**0.35**	**0.28**	**0.22**	**0.17**	**0.13**	**0.11**
IS	SRAM Cell (6-transistor) Area w/overhead (μm^2)++	**1.2**	**0.93**	**0.73**	**0.57**	**0.45**	**0.35**	**0.27**	**0.22**	**0.17**
IS	Logic Gate (4-transistor) Area (μm^2)++	**2.06**	**1.63**	**1.30**	**1.03**	**0.82**	**0.65**	**0.51**	**0.41**	**0.32**
IS	Logic Gate (4-transistor) Area w/overhead (μm^2)++	**4.1**	**3.3**	**2.6**	**2.1**	**1.6**	**1.3**	**1.03**	**0.82**	**0.65**
	Transistor density SRAM (Mtransistors/cm^2)	**504**	**646**	**827**	**1,057**	**1,348**	**1,718**	**2,187**	**2,781**	**3,532**
	Transistor density logic (Mtransistors/cm^2)	**97**	**122**	**154**	**194**	**245**	**309**	**389**	**490**	**617**
	Generation at introduction *	**p07c**	**p10c**	**p10c**	**p10c**	**p13c**	**p13c**	**p13c**	**p16c**	**p16c**
	Functions per chip at introduction (million transistors [Mtransistors])	**386**	**386**	**386**	**773**	**773**	**773**	**1546**	**1546**	**1546**
	Chip size at introduction (mm^2) ‡	**222**	**353**	**280**	**222**	**353**	**280**	**222**	**353**	**280**
	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	**174**	**219**	**276**	**348**	**438**	**552**	**696**	**876**	**1,104**
	Generation at production *	**p04c**	**p04c**	**p07c**	**p07c**	**p07c**	**p10c**	**p10c**	**p10c**	**p13c**
	Functions per chip at production (million transistors [Mtransistors])	**193**	**193**	**386**	**386**	**386**	**773**	**773**	**773**	**1546**
	Chip size at production (mm^2) §§	**111**	**88**	**140**	**111**	**88**	**140**	**111**	**88**	**140**
	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	**174**	**219**	**276**	**348**	**438**	**552**	**696**	**876**	**1,104**

Table 1h MPU (High-volume Microprocessor) Cost-Performance Product Generations and Chip Size Model—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	SRAM Cell (6-transistor) Area factor ++	104.1	103.4	102.8	102.2	101.7	101.3	100.9
	Logic Gate (4-transistor) Area factor ++	320	320	320	320	320	320	320
	SRAM Cell (6-transistor) Area efficiency ++	0.63	0.63	0.63	0.63	0.63	0.63	0.63
	Logic Gate (4-transistor) Area efficiency ++	0.50	0.50	0.50	0.50	0.50	0.50	0.50
IS	SRAM Cell (6-transistor) Area (μm^2)++	0.084	0.066	0.052	0.041	0.032	0.026	0.020
IS	SRAM Cell (6-transistor) Area w/overhead (μm^2)++	0.13	0.106	0.083	0.066	0.052	0.041	0.032
IS	Logic Gate (4-transistor) Area (μm^2)++	0.26	0.20	0.16	0.13	0.10	0.08	0.06
IS	Logic Gate (4-transistor) Area w/overhead (μm^2)++	0.51	0.41	0.32	0.26	0.20	0.16	0.13
	Transistor density SRAM (Mtransistors/cm^2)	4,484	5,687	7,208	9,130	11,558	14,625	18,497
	Transistor density logic (Mtransistors/cm^2)	778	980	1,235	1,555	1,960	2,469	3,111
	Generation at introduction *	p16c	p19c	p19c	p19c	p22c	p22c	p22c
	Functions per chip at introduction (million transistors [Mtransistors])	3092	3092	3092	6184	6184	6184	12368
	Chip size at introduction (mm^2) ‡	222	353	280	222	353	280	222
	Cost performance MPU (Mtransistors/cm^2 at introduction) (including on-chip SRAM) ‡	1,391	1,753	2,209	2,783	3,506	4,417	5,565
	Generation at production *	p13c	p13c	p16c	p16c	p16c	p19c	p19c
	Functions per chip at production (million transistors [Mtransistors])	1546	1546	3092	3092	3092	6184	6184
	Chip size at production (mm^2) §§	111	88	140	111	88	140	111
	Cost performance MPU (Mtransistors/cm^2 at production, including on-chip SRAM) ‡	1,391	1,753	2,209	2,783	3,506	4,417	5,565

Notes for Tables 1g and 1h:
++ The MPU area factors are analogous to the "cell area factor" for DRAMs. The reduction of area factors has been achieved historically through a combination of many factors, for example—use of additional interconnect levels, self-alignment techniques, and more efficient circuit layout. However, recent data has indicated that the improvement (reduction) of the area factors is slowing, and is virtually flat for the logic gate area factor.
** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p04c, was introduced in 2002, but not ramped into volume production until 2004; similarly, the p07c, is introduced in 2004, but is targeted for volume production in 2007.*
‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/2000), and the combination of both SRAM and logic transistor functionality doubles every technology node cycle.
§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.
Refer to the Glossary for definitions.

Table 1i High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Logic (Low-volume Microprocessor) High-performance ‡									
Generation at Introduction	**p07h**	**p10h**	**p10h**	**p10h**	**p13h**	**p13h**	**p13h**	**p16h**	**p16h**
Functions per chip at introduction (million transistors)	**1106**	**2212**	**2212**	**2212**	**4424**	**4424**	**4424**	**8848**	**8848**
Chip size at introduction (mm^2)	**492**	**781**	**620**	**492**	**781**	**620**	**492**	**781**	**620**
*Generation at production ***	**p04h**	**p04h**	**p07h**	**p07h**	**p07h**	**p10h**	**p10h**	**p10h**	**p13h**
Functions per chip at production (million transistors)	**553**	**553**	**1106**	**1106**	**1106**	**2212**	**2212**	**2212**	**4424**
Chip size at production (mm^2) §§	**246**	**195**	**310**	**246**	**195**	**310**	**246**	**195**	**310**
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	**225**	**283**	**357**	**449**	**566**	**714**	**899**	**1133**	**1427**
ASIC									
ASIC usable Mtransistors/cm^2 (auto layout)	**225**	**283**	**357**	**449**	**566**	**714**	**899**	**1,133**	**1,427**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	***858***	***858***	***858***	***858***	***858***	***858***	***858***	***858***	***858***
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**1,928**	**2,430**	**3,061**	**3,857**	**4,859**	**6,122**	**7,713**	**9,718**	**12,244**

Table 1j High-Performance MPU and ASIC Product Generations and Chip Size Model—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Logic (Low-volume Microprocessor) High-performance ‡							
Generation at Introduction	**p16h**	**p19h**	**p19h**	**p19h**	**p22h**	**p22h**	**p22h**
Functions per chip at introduction (million transistors)	**8848**	**17696**	**17696**	**17696**	**35391**	**35391**	**35391**
Chip size at introduction (mm^2)	**492**	**781**	**620**	**492**	**781**	**620**	**492**
*Generation at production ***	**p13h**	**p13h**	**p16h**	**p16h**	**p16h**	**p19h**	**p19h**
Functions per chip at production (million transistors)	**4424**	**4424**	**8848**	**8848**	**8848**	**17696**	**17696**
Chip size at production (mm^2) §§	**246**	**195**	**310**	**246**	**195**	**310**	**246**
High-performance MPU Mtransistors/cm^2 at introduction and production (including on-chip SRAM) ‡	**1798**	**2265**	**2854**	**3596**	**4531**	**5708**	**7192**
ASIC							
ASIC usable Mtransistors/cm^2 (auto layout)	**1,798**	**2,265**	**2,854**	**3,596**	**4,531**	**5,708**	**7,192**
ASIC max chip size at production (mm^2) (maximum lithographic field size)	***858***	***858***	***858***	***858***	***858***	***858***	***858***
ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)	**15,427**	**19,436**	**24,488**	**30,853**	**38,873**	**48,977**	**61,707**

Notes for Tables 1i and 1j:
** p is processor, numerals reflect year of production; c indicates cost-performance product. Examples—the cost-performance processor, p04c, was introduced in 2002, but not ramped into volume production until 2004; similarly, the p07c, is introduced in 2004, but is targeted for volume production in 2007.*
‡ MPU Cost-performance Model—Cost-performance MPU includes Level 2 (L2) on-chip SRAM (512Kbyte/2000), and the combination of both SRAM and logic transistor functionality doubles every technology cycle.

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.
Refer to the Glossary for definitions.

Table 2a Lithographic-Field and Wafer-Size Trends—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Lithography Field Size									
Maximum Lithography Field Size—area (mm^2)	**858**	**858**	**858**	**858**	**858**	**858**	**858**	**858**	**858**
Maximum Lithography Field Size—length (mm)	**33**	**33**	**33**	**33**	**33**	**33**	**33**	**33**	**33**
Maximum Lithography Field Size—width (mm)	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)									
Bulk or epitaxial or SOI wafer	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**450**	**450**

Table 2b Lithographic-Field and Wafer Size Trends—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Lithography Field Size							
Maximum Lithography Field Size—area (mm^2)	**858**	**858**	**858**	**858**	**858**	**858**	**858**
Maximum Lithography Field Size—length (mm)	**33**	**33**	**33**	**33**	**33**	**33**	**33**
Maximum Lithography Field Size—width (mm)	**26**	**26**	**26**	**26**	**26**	**26**	**26**
Maximum Substrate Diameter (mm)—High-volume Production (>20K wafer starts per month)							
Bulk or epitaxial or SOI wafer	**450**	**450**	**450**	**450**	**450**	**450**	**450**

Table 3a Performance of Packaged Chips: Number of Pads and Pins—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	Number of Chip I/Os (Number of Total Chip Pads)—Maximum									
	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072	3,072
	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024	1,024
	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048
	Total pads—ASIC high-performance	4,000	4,200	4,400	4,400	4,600	4,800	4,800	5,000	5,400
	Signal I/O pads—ASIC high-performance	2,000	2,100	2,200	2,200	2,300	2,400	2,400	2,500	2,700
	Power and ground pads—ASIC high-performance (½ of total pads)	2,000	2,100	2,200	2,200	2,300	2,400	2,400	2,500	2,700
	Number of Total Package Pins—Maximum [1]									
IS	Microprocessor/controller, cost-performance	550–900	550–1936	600–2140	600–2400	660–2801	660–2783	720-3061	720–3367	800–3704
IS	Microprocessor/controller, high-performance	3400	3800	4000	4400	4620	4851	5094	5348	5616
IS	ASIC (high-performance)	3400	3800	4000	4400	4620	4851	5094	5348	5616

Notes for Tables 3a and 3b:
[1] Pin counts will be limited for some applications where fine pitch array interconnect is used by printed wiring board (PWB) technology and system cost. The highest pin count applications will as a result use larger pitches and larger package sizes. The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4.

Table 3b Performance of Packaged Chips: Number of Pads and Pins—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	Number of Chip I/Os (Number of Total Chip Pads)—Maximum							
	Total pads—MPU	3,072	3,072	3,072	3,072	3,072	3,072	3,072
	Signal I/O—MPU (1/3 of total pads)	1,024	1,024	1,024	1,024	1,024	1,024	1,024
	Power and ground pads—MPU (2/3 of total pads)	2,048	2,048	2,048	2,048	2,048	2,048	2,048
	Total pads—ASIC high-performance	5,400	5,600	6,000	6,000	6,200	6,200	6,200
	Signal I/O pads—ASIC high-performance	2,700	2,800	3,000	3,000	3,100	3,100	3,100
	Power and ground pads—ASIC high-performance (½ of total pads)	2,700	2,800	3,000	3,000	3,100	3,100	3,100
	Number of Total Package Pins—Maximum [1]							
IS	Microprocessor/controller, cost-performance	800-4075	880–4482	880–4930	960-5423	960–5966	1050-6562	1050-7218
IS	Microprocessor/controller, high-performance	5896	6191	6501	6826	7167	7525	7902
IS	ASIC (high-performance)	5896	6191	6501	6826	7167	7525	7902

Table 4a Performance and Package Chips: Pads, Cost—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	Chip Pad Pitch (micron)									
	Pad pitch—ball bond [no update - deleted by A&P]	35	35	30	30	25	25	25	20	20
	Pad pitch—wedge bond	30	25	25	25	20	20	20	20	20
IS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	150	130	130	130	120	120	120	110	110
IS	Pad Pitch—2-row staggered-pitch (micron)	50	50	45	45	40	40	35	35	35
IS	Pad Pitch—Three-tier-pitch pitch (micron)	60	55	50	50	45	45	40	40	35
	Cost-Per-Pin									
IS	Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly – Cost-performance) — minimum–maximum	.67-1.17	.72-1.26	.69-1.19	.66-1.13	.63-1.70	.60-1.20	.57-.97	.54-.92	.51-.87
IS	Package cost (cents/pin) (Low-cost, hand-held and memory) — minimum–maximum	.27-.50	.28-.53	.27-.50	.25-.48	.24-.46	.23-.44	.22-.42	.21-.40	.20-.38

Table 4b Performance and Package Chips: Pads, Cost—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	Chip Pad Pitch (micron)							
	Pad pitch—ball bond [no update - deleted by A&P]	20	20	20	20	20	20	20
	Pad pitch—wedge bond	20	20	20	20	20	20	20
IS	Pad Pitch—area array flip-chip (cost-performance, high-performance)	100	100	95	95	90	90	85
IS	Pad Pitch—2-row staggered-pitch (micron)	35	35	35	35	35	35	35
IS	Pad Pitch—Three-tier-pitch pitch (micron)	35	35	35	35	35	35	35
	Cost-Per-Pin							
IS	Package cost (cents/pin) (Cost per Pin Minimum for Contract Assembly – Cost-performance) — minimum–maximum	.48 - .83	.46 - .79	.44 - .75	.42 - .71	.39 - .68	.37 - .64	.36 - .61
IS	Package cost (cents/pin) (Low-cost, hand-held and memory) — minimum–maximum	.20-.36	.20 -.34	.20-.32	.20-.30	.2-.29	.2-.27	.2-.26

Table 4c Performance and Package Chips: Frequency On-chip Wiring Levels—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
	Chip Frequency (MHz)									
	On-chip local clock [1]	**5,204**	**6,783**	**9,285**	**10,972**	**12,369**	**15,079**	**17,658**	**20,065**	**22,980**
IS	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[2]	**3,125**	**3,906**	**4,883**	**6,104**	**7,629**	**9,537**	**11,921**	**14,901**	**18,626**
IS	Maximum number wiring levels—maximum [3] **[**]**	**15**	**15**	**15**	**16**	**16**	**16**	**16**	**16**	**17**
IS	Maximum number wiring levels—minimum [3] **[**]**	**11**	**11**	**11**	**12**	**12**	**12**	**12**	**12**	**13**

Table 4d Performance and Package Chips: Frequency On-chip Wiring Levels—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	Chip Frequency (MHz)							
	On-chip local clock [1]	**28,356**	**33,403**	**39,683**	**45,535**	**53,207**	**62,443**	**73,122**
IS	Chip-to-board (off-chip) speed (high-performance, for peripheral buses)[2]	**23,283**	**29,104**	**34,925**	**41,910**	**50,291**	**60,350**	**72,420**
IS	Maximum number wiring levels—maximum [3] **[**]**	**17**	**17**	**17**	**18**	**18**	**18**	**18**
IS	Maximum number wiring levels—minimum [3] **[**]**	**13**	**13**	**13**	**14**	**14**	**14**	**14**

Note for Tables 4c and 4d:

[1] The on-chip frequency is based on the fundamental transistor delay (defined by the PIDS TWG), and an assumed maximum number of 12 inverter delays beginning 2007; after 2007, the PIDS model fundamental reduction rate of ~ -14.7% for the transistor delay results in a ~17.2% growth trend of the on-chip frequency through 2020;

[2] The off-chip frequency, as defined by the Assembly and Packaging model, increases at a growth trend of 25% through 2017, then crosses over the on-chip frequency. The off-chip frequency is expected to increase only for a small number of high-speed pins that will be used in combination with a large number of lower speed pins.

[3] The minimum number of wiring levels represents the interconnect metal levels, and the maximum number of interconnect wiring levels includes the Minimum number of wiring levels plus additional optional levels required for power, ground, signal conditioning, and integrated passives (i.e., capacitors).

*****: Interconnect table 81a&b is missing the # Metal Wiring Levels, and the "optional levels" (4) is incorrectly labeled as metal wiring levels]***

Table 5a Electrical Defects—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	23	20	18	16	14	13
WAS	DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	3,517	2,216	2,791	3,516	2,215	2,791	3,516	2,215	2,791
IS	DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	3517	3517	3517	2957	2957	2957	2957	2957	2957
WAS	MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	1,757	2,214	1,395	1,757	2,214	1,395	1,757	2,214	1,395
IS	MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	1395	1395	1395	1395	1395	1395	1395	1395	1395
	# Mask Levels—MPU	33	33	33	35	35	35	35	35	37
	# Mask Levels—DRAM	24	24	24	24	24	26	26	26	26

Table 5b Electrical Defects—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
WAS	DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	3,516	2,215	2,791	3,516	2,215	2,791	3,516
IS	DRAM Random Defect D_0 at production chip size and 89.5% yield (faults/m^2) §	2957	2957	2957	2957	2957	2957	2957
WAS	MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	1,757	2,214	1,395	1,757	2,214	1,395	1,757
IS	MPU Random Defect D_0 at production chip size and 83% yield (faults/ m^2) §§	1395	1395	1395	1395	1395	1395	1395
	# Mask Levels—MPU	37	37	37	39	39	39	39
	# Mask Levels—DRAM	26	26	26	26	26	26	26

Notes for Tables 5a and 5b:

D_0 — defect density

§ DRAM Model—Cell Area Factor (design/process improvement) targets are as follows:

1999–2007/8×: 2008-2020/6×. Due to the elimination of the "7.5," "7," and the "5" DRAM Cell design improvement Factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the latest model 2005 ITRS timeframe:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.

Refer to the Glossary for definitions.

Table 6a Power Supply and Power Dissipation—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Power Supply Voltage (V)									
Vdd (high-performance)	**1.1**	**1.1**	**1.1**	**1.0**	**1.0**	**1.0**	**1.0**	**0.9**	**0.9**
V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.9**	**0.9**	**0.8**	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.6**
Allowable Maximum Power [1]									
High-performance with heatsink (W)	**167**	**180**	**189**	**198**	**198**	**198**	**198**	**198**	**198**
Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	**310**	**310**	**310**	**310**	**310**	**310**	**310**	**310**	**310**
Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	**0.54**	**0.58**	**0.61**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**
Cost-performance (W)	**91**	**98**	**104**	**111**	**116**	**119**	**119**	**125**	**137**
Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**	**140**
Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	**0.65**	**0.70**	**0.74**	**0.79**	**0.83**	**0.85**	**0.85**	**0.89**	**0.98**
Battery (W)—(low-cost/hand-held)	**2.8**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 6b Power Supply and Power Dissipation—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	Power Supply Voltage (V)							
	Vdd (high-performance)	**0.9**	**0.8**	**0.8**	**0.7**	**0.7**	**0.7**	**0.7**
	V_{dd} (Low Operating Power, high V_{dd} transistors)	**0.6**	**0.6**	**0.5**	**1.0**	**0.5**	**0.5**	**0.5**
	Allowable Maximum Power [1]							
	High-performance with heatsink (W)	**198**	**198**	**198**	**198**	**198**	**198**	**198**
	Maximum Affordable Chip Size Target for High-performance MPU Maximum Power Calculation	**310**	**310**	**310**	**310**	**310**	**310**	**310**
	Maximum High-performance MPU Maximum Power Density for Maximum Power Calculation	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**	**0.64**
IS	Cost-performance (W)	**137**	**137**	**151**	**151**	**151**	**151**	**151**
	Maximum Affordable Chip Size Target for Cost-performance MPU Maximum Power Calculation	**140**	**140**	**140**	**140**	**140**	**140**	**140**
IS	Maximum Cost-performance MPU Maximum Power Density for Maximum Power Calculation	**0.98**	**0.98**	**1.08**	**1.08**	**1.08**	**1.08**	**1.08**
	Battery (W)—(low-cost/hand-held)	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**	**3.0**

[1] Power will be limited more by system level cooling and test constraints than packaging

Table 7a Cost—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
Affordable Cost per Function ++									
DRAM cost/bit at (packaged microcents) at samples/introduction	**5.3**	**3.7**	**2.6**	**1.9**	**1.3**	**0.93**	**0.66**	**0.46**	**0.33**
DRAM cost/bit at (packaged microcents) at production §	**1.9**	**1.4**	**0.96**	**0.68**	**0.48**	**0.34**	**0.24**	**0.17**	**0.12**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**44.0**	**31.1**	**22.0**	**15.6**	**11.0**	**7.8**	**5.5**	**3.9**	**2.8**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**26.6**	**18.8**	**13.3**	**9.4**	**6.7**	**4.7**	**3.3**	**2.4**	**1.7**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**24.4**	**17.2**	**12.2**	**8.6**	**6.1**	**4.3**	**3.0**	**2.2**	**1.5**

Table 7b Cost—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (f)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Affordable Cost per Function ++							
DRAM cost/bit at (packaged microcents) at samples/introduction	**0.23**	**0.16**	**0.12**	**0.08**	**0.06**	**0.04**	**0.03**
DRAM cost/bit at (packaged microcents) at production §	**0.08**	**0.06**	**0.04**	**0.03**	**0.02**	**0.01**	**0.01**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at introduction §§	**1.9**	**1.4**	**0.97**	**0.69**	**0.49**	**0.34**	**0.24**
Cost-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**1.2**	**0.83**	**0.59**	**0.42**	**0.29**	**0.21**	**0.15**
High-performance MPU (microcents/transistor) (including on-chip SRAM) at production §§	**1.1**	**0.76**	**0.54**	**0.38**	**0.27**	**0.19**	**0.13**

Notes for Tables 7a and 7b:

++ Affordable packaged unit cost per function based upon average selling prices (ASPs) available from various analyst reports less gross profit margins (GPMs); 35% GPM used for commodity DRAMs and 60% GPM used for MPUs; 0.5×/two years inTER-generation reduction rate model used; .55×/year inTRA-generation reduction rate model used; DRAM unit volume life-cycle peak occurs when inTRA-generation cost per function is crossed by next generation, typically seven–eight years after introduction; MPU unit volume life-cycle peak occurs typically after four–six years, when the next generation processor enters its ramp phase (typically two to four years after introduction).

§ DRAM Model—cell area factor (design/process improvement) targets are as follows:

1999–2007/8×: 2008-2020/6×. Due to the elimination of the "7.5," "7," and the "5" DRAM cell design improvement factors [a] in the latest 2005 ITRS DRAM consensus model, the addition of "Moore's Law" bits/chip slows from 2× every 2.5–3 years to 2× every three years.

DRAM product generations were increased by 4× bits/chip every four years with interim 2× bits/chip generation. However, in the latest model 2005 ITRS timeframe:

1. at the Introduction phase, after the 16 Gbit generation, the introduction rate is 4×/six years (2×/three years); and

2. at the Production phase, after the 4 Gbit generation, the introduction rate is 4×/six years (2×/three years).

As a result of the DRAM consensus model changes for the 2005 ITRS, the InTER-generation chip size growth rate model target for Production-phase DRAM products remains "flat" at less than 140 mm^2, similar to the MPU model. However, with the elimination of some of some of "cell area factor" reductions, the flat-chip-size model target requires the bits/chip "Moore's Law" model for DRAM products to increase the time for doubling bits per chip to an average of 2× per 3 years (see ORTC Table 1c and d).

Furthermore, the cell array efficiency (CAE – the Array % of total chip area) was corrected to 56.1% after 2008, since only the storage cell array area benefits from the 6× "cell area factor" improvement, not the periphery. This CAE change in the model puts even additional pressure on the Production-phase product chip size to meet the target flat-chip-size model. It can be observed in the latest table 1c and d model data that the InTRA-generation chip size shrink model is still 0.5× every technology cycle (to 0.71× reduction) in-between cell area factor reductions.

18 Overall Roadmap Technology Characteristics

§§ MPU Chip Size Model—Both the cost-performance and high-performance MPUs InTER-generation production-level chip sizes are modeled to be below affordable targets, which are flat through 2020 (280 mm^2/cost-performance at introduction; 140 mm^2/cost-performance at production; 310 mm^2/high-performance at production). The MPU flat chip-size affordability model is accomplished by doubling the on-chip functionality every technology node cycle. Actual market chip sizes may exceed the affordability targets in order to continue the doubling of on-chip functionality on a shorter cycle, but their unit costs and market values must be increased. In the 2005 ITRS, the MPU model now includes introduction-level high-performance MPU targets that shrink to the "affordable" targets (the same way the DRAM model operates). The InTRA-generation chip size shrink model is 0.5× every two-year density-driven technology cycle through 2004, and then 0.5× every three-year density-driven technology cycle after 2004, in order to stay under the affordable flat-chip-size target.
Refer to the Glossary for definitions.

2006 UPDATE: WORKING GROUP SUMMARIES

SYSTEM DRIVERS

The 2006 update of the System Drivers Chapter is a step in the direction of market-driven drivers that reflect the demands of a 21st-century roadmap. Driving towards the 2007 version of the roadmap, the set of main drivers is moving towards becoming a market-driven set, including driver segments such as office, consumer mobile drivers. This year one more driver is added, the consumer stationary driver that represents a high-performance version of the increasingly important consumer electronics market. Other existing drivers have been reviewed to ensure the direction is appropriate. A complete set of market-driven drivers is expected for the 2007 version of the System Drivers roadmap, for which the plan is on track.

DESIGN

After going through a major overhaul in the 2005 version, the 2006 design chapter update now features a full quantitative design technology roadmap. This year's update has focused primarily on providing meaningful updates of some of the figures, dates, and challenge items provided, including moderate revisions of the System-Level and Verification Sections and minor revisions of the rest of the sections. An increasing number of sections includes a table that relates challenges and solutions. Although a one-on-one relationship is usually not warranted, it is quite helpful in certain parts of the design flow. The 2007 version of this chapter will continue in this direction while increasingly accounting for alternative integration methods that add on to Moore's Law (heterogenous systems, system-in-packege (SIP), etc.).

TEST AND TEST EQUIPMENT

The 2006 update to the ITRS Test Chapter is focused on minor corrections to previously published trend information. Corrections occurred to the Multi-Site wafer probing table where the parallelism for low performance microcontrollers was reduced. The Multi-Site efficiency numbers for the long-term years 2014 thru 2020 were omitted in the 2005 roadmap and have been included in the 2006 tables. NAND wafer and packaged unit test parallelism roadmap has been pulled in by 2 years and the NAND roadmap has been updated to reflect a higher bus performance starting in 2010. The system-oc-chip (SOC) roadmap reflects a push out of some defect models and analog test standards as progress in these areas have not kept up with the previous forecast. The mixed signal bandwidth and sampling rate roadmaps have been pulled in by a couple of years. This update does not identify any fundamental changes to the industry roadmap.

The 2005 roadmap did not contain the definitions of high, medium, or low “performance” for the various device types included in the tables. For the 2006 update, low end logic devices have fewer than 150 signal pins and an I/O bit rate of less than 400 Mbps. High performance Flash has an I/O bit rate of greater than 125 Mbps. The definition of performance is not static and should change over the duration of this roadmap. A table for high, medium, and low end performance will be further included in 2007 roadmap.

2007 international technology working group (ITWG) activities are focused on refining the full 2005 chapter rewrite and fleshing out areas that were not fully addressed. The rapid adoption of system-in-package (SIP), SOC, and NAND devices has been driving some trends faster than expected, which has resolved some difficult challenges but created others that will require new methodology such as testing SIP die “hidden” by other die.

PROCESS INTEGRATION, DEVICES AND STRUCTURES

The 2006 PIDS chapter is mainly unchanged from the 2005 edition. There are minor updates and corrections, but major changes will await the 2007 edition. The exception is in the Logic Technology Requirements tables, where there are notable changes in the timing of the projected deployment of several key technology innovations. Specifically, for high-performance and low operating power (LOP) logic, the projected implementation of high-κ gate dielectric and metal gate electrode is delayed from 2008 (as forecasted in the 2005 ITRS) until 2010. Also, the projected implementation of fully depleted ultra-thin body (FD-UTB) silicon-on-insulator (SOI) MOSFETs for high-performance logic is delayed from 2008 (as forecasted in the 2005 ITRS) until 2010. The reason for these delays is that it now seems unlikely that the integrated circuit (IC) industry will find it feasible to deploy these innovations as early as 2008. However, for low standby power (LSTP) logic, the projected implementation of high-κ gate dielectric and metal gate electrode is in 2008, as forecasted in the 2005 ITRS. For LSTP, the relatively thick dielectric equivalent oxide thickness of 1.6 nm in 2008 and the potential use of fully silicided gate electrodes make the 2008 projected deployment more feasible than for LOP and high-performance logic.

The consequences of the delay in deploying high-κ gate dielectric and metal gate electrode were analyzed for the affected years, 2008 and 2009. The scaling of the equivalent oxide thickness of the gate dielectric is slowed in 2008 and 2009 compared to that in the 2005 PIDS tables in order to keep the gate leakage current within tolerable limits. Other consequences for those two years include increases in the source/drain leakage current and some slowing in the scaling of the transistor intrinsic delay, τ. Furthermore, $\tau = CV_{dd}/I_{d,sat}$, where C is the load capacitance, V_{dd} is the power supply voltage, and $I_{d,sat}$ is the transistor saturation drive current. Since C is inversely proportional to the equivalent oxide thickness, both C and $I_{d,sat}$ are reduced for 2008 and 2009. See the text and the updated technology requirements tables for details.

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES FOR WIRELESS COMMUNICATIONS

STATE OF WIRELESS TECHNOLOGIES 2006—ITRS PERSPECTIVE

Radio frequency (RF) and analog mixed-signal technologies serve the rapidly growing wireless communications market and represent essential and critical technologies for the success of many semiconductor manufacturers. Communications products may replace computers as a key driver of volume manufacturing. Consumer products now account for over half of the demand for semiconductors.[1] For example, third generation (3G) cellular phones now have a much higher semiconductor content and now are 50 % of the cellular phone market compared to only 5 % of the market a few years ago. The consumer portions of wireless communications markets are very sensitive to cost. With different technologies capable of meeting technical requirements, time to market and overall system cost will govern technology selection.

The boundary between silicon-based and III-V semiconductors continues to move to higher frequencies with time. Frequency will be less important for defining the boundaries among technologies and other parameters such as noise figure, output power, power-added efficiency, linearity and ultimately cost will become more important. This shift in importance from frequency to parameters such as those listed in the previous sentence is already occurring for power amplifiers.

For CMOS, the long term prediction of device RF and noise performance becomes more uncertain with the introduction of metal gate electrodes (2009), high permittivity (high-κ) gate dielectrics (2009), and new device structures such as fully depleted and/or double-gated silicon-on-insulator (SOI) (2015). The trend of higher integration and performance levels for logic with mixed-signal circuitry leads to steadily increasing digital processing capabilities that enable more signal treatments to be done in the digital domain.

For bipolar, the key driving forces include speed, power consumption, noise, and breakdown.

For passive devices, the biggest challenges are integrating them into a digital CMOS process and the trade-off between processing cost and device performance.

For power amplifiers—mobile, the nearly fixed battery voltages and ruggedness requirements tend to slow technology evolution. Highly integrated modules with multi-layer laminates are dramatically reducing total RF front end area.

[1] *P. H. Singer, "Dramatic Gains in Performance on the Horizon," editorial in* Semiconductor International*, Vol. 29, No. 8, 29, July 2006, page 15.*

For power amplifiers—basestation, the device cost is projected to steadily decrease from about $0.70/Watt today to less than $0.50/Watt by 2008 and the applications space is moving from 2 GHz and below to higher frequencies, such as worldwide interoperability for microwave access (WiMAX) at 3.5 GHz and from saturated power amplifiers to more linear amplifiers to support code division multiple access (CDMA) and wideband CDMA (WCDMA).

For millimeter wave applications, InP-based RF transistors have demonstrated very high frequencies and GaN transistors have demonstrated record power densities at 40 GHz of 10W/mm with 40 Volts drain bias. GaN is advancing much more quickly than predicted in 2003 and 2004.

Future wireless challenges include signal isolation and the software defined radio (SDR). A signal isolation roadmap with quantitative technical requirements is very difficulty because agreement on which figures of merit and measurements to use does not exist. The SDR presents many issues such as the analog-to-digital (ADC) performance, transmitter solutions, and cost.

EMERGING RESEARCH DEVICES

The teams for Emerging Research Devices, including Emerging Research Materials, were very active in 2006, preparing for the complete revision of the material in 2007. Updates and changes are deferred until the 2007 ITRS.

FRONT END PROCESSES

Updates to the Front End Processes (FEP) chapter in 2006 have been minimal except in the area of thermal/thin films (see below). A few changes have been made to the FEP Difficult Challenges, Table 66a and Table 66b. In Table 66a we recognize that local strain has been integrated into current IC manufacturing and should be extendable to at least the 32 nm generation. In Table 66b we note that continued scaling of local strain will be a challenge beyond the 32 nm generation. We also note that implementation of high-κ gate stack materials in low standby power (LSTP) applications should be achievable, while implementation of these materials in high performance (HP) logic and low operating power (LOP) applications is still considered a difficult challenge. Introduction of 450 mm wafers in 2012 is still considered a difficult challenge facing numerous issues.

In the Starting Materials and Surface Preparation sections of this chapter we included a few minor updates in the color indications. Starting Materials particle metrics for 2011 have been changed from yellow to white and Surface Preparation material loss metrics for 2008 and beyond have been changed from red to "interim solutions are known". In the Surface Preparation Potential Solutions chart, Figure 57, we have indicated a delay in the potential introduction of supercritical CO_2 methods to manufacturing.

Updates for Thermal/Thin Films, Doping and Etching are centered on the timing for introduction of high-κ/metal advance gate stack materials and also for introduction of fully depleted silicon on insulator (FDSOI). The updates to Table 69a reflect a push back of the introduction of advanced gate materials for HP logic and for LOP to the year 2010. The introduction of advanced gate stack materials for LSTP remains in 2008. Also, the introduction of FDSOI for HP logic has been pushed back to 2010. These changes for advanced gate stack and FDSOI were made after extensive discussion with the Process Integration, Devices, and Structures (PIDS) Technology Working Group (TWG) and reflect the expected readiness of these new materials for commercial production.

For dynamic random access memory (DRAM) Stacked Capacitor we have made some changes in the potential solutions chart, Figure 61, for high-κ materials. For DRAM Trench Capacitor the use of NO dielectric has been extended through the 70 nm generation, with high-κ materials being introduced at the 65 nm generation. In addition, for the DRAM Trench Capacitor new integration schemes to be introduced at 40 nm will reduce the thermal budget for the cell capacitor. Thus a more aggressive scaling of the capacitance equivalent oxide thickness (CET) will be possible. As a consequence the trench aspect ratio can be kept at less than 100 down to the 28 nm generation.

For Flash Non-Volatile Memory a new row has been added to Table 72 for the "STI Filling Aspect Ratio". A footnote has also been added to Table 72 to explain this new row. For Phase Change Memory (PCM) a new table has been introduced to indicate two important metrics for PCM scaling: phase change material conformality and minimum operating temperature.

Finally, for ferroelectric RAM (FeRAM), a note has been added about the implementation issues with BFO ($BiFeO_3$) and other ferroelectric materials. In addition the FeRAM Potential Solutions chart, Figure 65, has been updated to include BFO.

LITHOGRAPHY

The following updates were made to the Lithography chapter for 2006:

DIFFICULT CHALLENGES

- Double exposure / patterning
  - Overlay of multiple exposures including mask image placement
  - Availability of software to split the pattern apply optical proximity correction (OPC), and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
  - Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
  - Photoresists with independent exposure of multiple passes
  - Fab logistics and process control to enable low cycle time impact that include on-time availability of additional reticles and efficient scheduling of multiple exposure passes

TECHNOLOGY REQUIREMENTS

- Mask tables
  - Color changes only: based on improvements in the industry
    - Optical mask tables, extreme ultra-violet lithography (EUVL) mask tables, and imprint template tables
  - Added lines for double exposure (mask image placement and mask critical dimension (CD) mean)
  - Corrected data volume values for EUVL
- Resist tables
  - Added lines for defects in double exposure processes
- Maskless lithography
  - Two lines added for grid size and data volume

POTENTIAL SOLUTIONS

- 45nm
  - 193i/H_2O
  - ADDED 193i double patterning
  - 193i with other fluids
  - EUV, maskless lithography (ML2)
- 32nm
  - EUV
  - ADDED 193i double patterning
  - 193i with other fluids and lens materials
  - ML2, Imprint
- 22/16nm
  - No dramatic changes

Changed order of ML2, Imprint

INTERCONNECT

It should be noted that for the 2006 ITRS Interconnect roadmap, the title of the primary technology requirements table has been expanded to include ASICs and is now "MPU and ASIC Interconnect Technology Requirements."

Also for 2006, in recognition of the increasing importance of the dynamic power dissipated in the interconnect structure, a new power metric has been added to the MPU and ASIC Technology Requirements Tables. The power metric is the power (measured in Watts) dissipated per Ghz of frequency and cm^2 of metal layer. The power metric is shown as a range for each of the roadmap years. Although the power metric is seen to plateau for the long-term years due to aggressive introduction of low-κ dielectrics, the power dissipated in the interconnect structure will still increase dramatically due to higher frequencies and increases in the number of metal layers. Note that this metric is a measure of the dynamic power associated with the interconnect structure and the actual power dissipation of a specific MPU or ASIC will be a function of architecture and implementation of power saving design features. This power metric will also serve as a key benchmark so that future interconnect alternatives, such as radio frequency (RF), optical or carbon nanotubes, can be compared to conventional wiring technology.

In addition to the power metric, the capacitance per unit length for Metal 1, intermediate, and minimum global wiring layers has also been added to the tables for 2006. The Cu resistivity of these layers had been added in prior years and with the addition of capacitance, the RC values can easily be calculated.

The metric for Interlevel-metal insulator–bulk dielectric constant (κ) has also been changed for 2006. In prior roadmaps, this metric had been listed as the minimum expected for each year. This metric has been replaced with a range of values depicting both the most aggressive bulk dielectric constant expected as well as a more realistic case. This range of bulk κ values was then used to calculate the metric which lists the range of κ_{eff} values for each of the roadmap years.

One of the grand challenges for interconnect is the result of the rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity. These create integration, cost, and reliability challenges.

Another of the grand challenges is the variability associated with line edge roughness, trench and via depth and profile, etch bias, thinning due to cleaning and CMP as well as size effects.

Traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low κ will require material innovation, combined with accelerated design, packaging and unconventional interconnect.

FACTORY INTEGRATION

SUMMARY

The 2006 Factory Integration section of the ITRS focuses on integrating all the factory components that are needed to efficiently produce the required products on schedule and in the right volumes while meeting cost targets. Realizing the potential of Moore's Law requires taking full advantage of device feature size reductions, new materials, yield improvement to near 100%, wafer size increases, other manufacturing productivity improvements and preserving the decades-long trend of 30% per year reduction in cost per function. To continue this pace requires the vigorous pursuit of the following fundamental manufacturing attributes: maintaining cost per unit area of silicon, decreasing factory ramp time, and increasing factory flexibility to changing technology and business needs.

Factory Integration addresses several challenges that threaten to slow the industry's growth, including:

1. Integrating complex business models with complex factories—Rapid changes in semiconductor technologies, business requirements, and the need for faster product delivery, high mix, and volatile market conditions are making it difficult for factories to effectively meet accelerated ramp and yield targets over time.
2. Production equipment reliability, utilization, and extendibility—Production equipment must keep up with availability and utilization targets, which has an enormous impact on capital and operating costs.
3. Maturing 300mm factory challenges— The semiconductor industry is now focusing on maturity of 300mm factories and hence 300mm efficiency must be improved and sustained while improving cost and cycle time targets. The ever-exploding factory data quantity and complexity need to be addressed as well.

4. Post Bulk CMOS and next wafer size manufacturing paradigm—Conversion to novel devices and the 450mm wafers represent key inflection points for semiconductor manufacturing and represents another opportunity to improve manufacturing cost effectiveness and the industry's ability to continue realizing Moore's law.

WHAT'S NEW FOR FACTORY INTEGRATION IN 2006?

The Factory Integration team completed minor updates to Operations, Equipment, Information & Control, AMHS and Facilities technology requirements tables. These changes corrected some of the errors from 2005 and also updated metric values that reflect the collective input from various members.

The team also worked on key focus areas such as: a) 300 Prime/450mm—defining requirements, constraints, partnerships with other efforts and timing, including, 300 Prime—to ensure current 300mm install base productivity improvements; b) proactive visualization—definition, impact due to high mix and small lot, factory metrics, intrinsic equipment loss through B/A metric and cycle time; c) design for facilities—adapter plate, power and water usage; d) equipment sleep mode—efforts kicked off to conserve power and time synchronization for factory applications.

In addition, Factory Integration worked with several other technology working groups (TWGs): Lithography, Front End Processes (FEP), Environment, Safety, & Health (ESH), Yield Enhancement, Assembly & Packaging, Test, Interconnect, and Metrology on cross-cut issues. Key topics were: extreme ultraviolet lithography (EUVL) requirements, the green fab initiative, 1.5mm wafer edge exclusion, adapter plate, fab humidity control, and single wafer versus batch processing for thermal processes and 450mm cross-cut issues.

In 2007, the Factory Integration team will continue to work on technology requirements, potential solutions (several updates were proposed in 2006 but are planned for insertion in 2007 since the team is working on supporting materials). The team will continue to work on key focus areas and with cross TWGs to address cross-cut issues in order to develop cogent technology requirements and potential solutions to enable our factories to effectively address the next business/manufacturing/technology challenges.

ASSEMBLY AND PACKAGING

The pace of change in assembly and packaging has accelerated as packaging is increasingly a limiting factor for both product cost and performance. Many of the tables have been updated to reflect these rapid changes. The major changes include:

The Difficult Challenges (Table 93) were amended to add issues associated with very small and very high frequency integrated circuits and the rapidly emerging requirements for packaging very thin die.

Extensive revisions in Tables 94 reflect changes in the projected technologies for chip to package interconnect. New entries were added for complex ICs in harsh environments since packageing requirements in this category can not be adequately covered by the existing categories.

The Materials Challenges (Table 95) update reflects the impact of changes in government regulations and the impact of demand for every thinner packages to accommodate requirements of portable consumer products.

Chip to Package Substrates (Table 96) have tape-automated bonding added reflecting the solder bump flip chip technology providing cost/performance advantages in spcific packaging applications.

Package Substrate Physical Properties (Table 98) have been updated to incorporate additional parameters for thermal properties that are increasingly critical for higher temperature, smaller form factor packages.

ENVIRONMENT, SAFETY, AND HEALTH

For 2005 the *ESH chapter* has been fully reorganized following a major revision of the ESH Difficult Challenges that now address the four categories: Chemicals and Materials Management, Process and Equipment Management, Facilities Energy and Water Optimization, and Sustainability and Product Stewardship. The revised Difficult Challenges are now more reflective of their multiple functions to be able to incorporate external influences (e.g., regulatory) on semiconductor technology development, serve as a more effective "filter" to evaluate the technology thrust needs, and identify intrinsic needs for ESH R&D. There has been further elimination of repetitive technical requirements that are considered ESH maintenance of business such as tool safety audits, which do not themselves require development, but are a method used

to evaluate tools entering the marketplace. Increasing emphasis has been placed on the need to understand and manage materials and material alternatives, given the growth in public policy concern over use of chemicals for which little ESH characterization is available. In addition, Product Stewardship has been formerly identified as an ESH challenge with appropriate technical requirements, as there grows increasing emphasis in the market over reducing hazardous content of products.

The 2006 Update revisions to the Environment, Safety, and Health chapter were minor and are summarized as follows. Roman numerals were added in Tables 104a & b, *ESH Intrinsic Requirements*, to indicate the major headings and distinguish them from sub-section titles. In Tables 105a & b, the word "lowest" (regarding ESH impact) was replaced with "low", indicative of the ever-changing nature of process materials and their critical process performance requirements. Additionally, a footnote was added to these tables to show mathematically the definition for the word "utilization", as used in the text. The title of Tables 106a & b was changed to align with the categories in Table 103, *ESH Difficult Challenges.* Also, minor changes were made to the wording around "idle water and energy usage". The last change worth noting included the addition of "Optimization of CMP Water Use at Idle" as a potential ESH solution in Figure 100.

YIELD ENHANCEMENT

The Yield Enhancement ITWG updated the tables regarding the topics Defect Budget and Yield Model, Defect Detection and Characterization and Wafer Environment and Contamination Control for the 2006 electronic update. The key challenges remain similar as 2005. The most important challenge will be the signal-to-noise ratio for defect inspection tools. Currently, inspection systems are expected to detect defects of sizes scaling down in the same way or even faster as feature sizes requested by technology generations. Increasing the inspection sensitivity at the same time increases the challenge to find small but yield-relevant defects under a vast amount of nuisance, false defects. In parallel a low cost of ownership of the tools demands for high throughput inspection.

Other topics challenging the Yield Enhancement community are prioritized as follows:

- *High Throughput Logic Diagnosis Capability*—identification and tackling of systematic yield loss mechanisms.
- *Detection of Multiple Killer Defect Types*—and simultaneous differentiation at high capture rates, low cost of ownership and throughput.
- *High-Aspect-Ratio Inspection*—need for high-speed and cost-effective high aspect ratio inspection tools remains as the work around using e-beam inspection does not at all meet requirement for throughput and low cost.
- *Process Stability vs. Absolute Contamination Level Including the Correlation to Yield*—data, test structures, and methods are needed for correlating process fluid contamination types and levels to yield and determine required control limits.
- *In-line Defect Characterization and Analysis*—as an alternative to EDX analysis systems. The focus is on light elements, small amount of samples due to particle size and microanalysis
- *Wafer Edge and Bevel Control and Inspection—i*n order to find the root cause inspection of wafer edge, bevel and apex on front and backside is needed
- *Data Management and Test Structures for Rapid Yield Learning*—to enable the rapid root-cause analysis of yield-limiting conditions
- *Development of Parametric Sensitive Yield Models*—including new materials, (OPC) – optical proximity correction and considering the high complexity of integration

The Yield Enhancement chapter consists of four subchapters as Yield Learning, Defect Budget and Yield Model, Defect Detection and Characterization, and Wafer Environment and Contamination Control. The major work during 2006 was the control and update of the tables. The changes summarizes as follows:

DEFECT BUDGET AND YIELD MODEL

This update includes standardization of chip size for PWP calculation and correction of unmarked errors. Additionally, 'Ymaterial' is newly introduced to separate starting material based yield degradation from process based one. It is a solution against modification of yield equation previously proposed by FEP ITWG.

DEFECT DETECTION AND CHARACTERIZATION

The table 113 was checked carefully against latest developments for defect inspection and detection. Discussions and adjustments regarding the estimation of impact of roughness on non patterned inspection and definitions for coordinate precision were performed.

WAFER ENVIRONMENT AND CONTAMINATION CONTROL

Table 115 has been updated especially in discussions with Lithography and Front-end processing working groups. It needs to be considered that the table does not only consider contaminations but also wafer environment process variables, which can be yield determining similar to contaminants. New process materials will continue to drive the list of ionic and other elemental impurities to be specified and monitored. Accurate liquid particle measurements continue to be a challenge at current and future device geometries. Organic contaminations require continued attention since many parameters used to specify and monitor are still not specific enough and do not pinpoint the contamination mechanisms clearly enough.

METROLOGY

During 2006, participation in the Metrology TWG increased. Supplier representation became more visible, and those members provided key insight for the group. Some of the changes initiated in 2006 will receive addition scrutiny in 2007, especially the impact of dual patterning on metrology. Changes in wafer level lithography metrology for CD were based on recent data showing in increased capability of CD metrology. Tightened tolerances for overlay indicate the need for acceleration of improvements in overlay metrology. In addition, the uncertainty associated with the timing of dual patterning combined with the lack of metrology for dual patterning a significant issue. Changes in the timing of the introduction of high κ and low κ change the timing of some metrology requirements.

MODELING AND SIMULATION

Similar to the other chapters of the ITRS, in the Modeling and Simulation chapter only the tables have been revised in the 2006 Update. Important other developments like the further increasing interdependencies with the other chapters of the ITRS, e.g., concerning Design for Manufacturing, have been discussed but can and will only be presented in the next full version of the ITRS in 2007. This is intended to further promote the usefulness of Modeling and Simulation to improve the physical understanding in semiconductor technology and to reduce development times and costs.

Concerning the Modeling and Simulation challenges, only some details of the six short-term and the four long-term challenges for Modeling and Simulation were changed: Concerning the short-term challenges, lithography simulation was extended by the inclusion of multiple exposure/patterning, which has during the last months got high and urgent interest to enable the printing of smaller feature sizes. Electromagnetic field effects have been explicitly mentioned because their accurate treatment is getting indispensable for sufficiently accurate simulation. Ultimate nanoscale CMOS simulation capability was extended by the explicit inclusion of novel memory devices, such as magnetic RAM (MRAM) and programmable RAM (PRAM). Furthermore, reliability modeling for ultimate CMOS has been highlighted. Thermal-mechanical-electrical modeling for interconnections and packaging was extended to include 3D integration. Concerning the long-term challenges, nanoscale modeling was extended to explicitly include non-charge state devices, which are in detail discussed in the Emerging Research Devices (ERD) section of the ITRS. Optoelectronics modeling was extended to include optical couplers.

Whereas the fields of requirements have not changed, several details, including some timelines, were modified or added in view of the changes in industrial needs and state-of-the-art. Among the most significant changes is the more detailed requirement on the lithography options, referring especially to the several upcoming generations of immersion lithography. The newly required multiple exposure option especially affects resist modeling. For device modeling, updates refer especially to (quasi-)ballistic transport and quantum effects.

As with the long-term challenges, the long-term requirements interactions with the ERD and Emerging Research Materials (ERM) part of the ITRS increasingly get important. In the 2006 update this has been documented among others by the inclusion of ERD devices in the long-term requirements for Numerical Device Simulation.

Concerning the Modeling and Simulations requirements tables, an important change has been the separation between the absolute accuracy of a model or simulator (after calibration to a certain technology, e.g., one company's 90 nm technology), and the accuracy of the sensitivity w.r.t. technological input parameters: for example, if the critical dimension (CD) of a gate is changed due to a change in exposure dose, that CD change should be predicted by simulation with an error of less than 10%.

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (WITH OBSERVATIONS AND ANALYSIS)

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets. MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

Example: DRAM half pitches of 180 nm, 130 nm, 90 nm, 65 nm, 45 nm, 32 nm, and 22 nm.

Moore's Law—An historical observation by Intel executive, Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that MPU performance [clock frequency (MHz) × instructions per clock = millions of instructions per second (MIPS)] also doubles every 1.5 to 2 years. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 30 years.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to Moore's Law, there is a historically-based "corollary" to the "law," which suggests that to be competitive manufacturing productivity improvements must also enable the cost-per-function (microcents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 1.5 years, then cost-per-chip (packaged unit) could double every six years and still meet the cost-per-function reduction requirement. If functionality doubles only every three years, as suggested by consensus DRAM and MPU models of the 2005 ITRS, then the manufacturing cost per chip (packaged unit) must remain flat.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two (L2) cache (example 1 Mbytes/2001). Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71x/cycle period) generation.

High-performance MPU—MPU product optimized for maximum system performance by combining a single or multiple CPU cores (example two cores at 25 Mt cores in 2002) with a large (example 4 Mbyte/2002) level-two (L2) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The present 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip has increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is required due to the new consensus 2005 ITRS forecast of cell-area-factor improvement to 6 by 2008, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate (virtually no design-related improvement). Therefore, the 2005 ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The 2003 ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology node processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology node, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples. Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2003 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (<1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, at least 10K/month) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume

production ramp. Beta-level tools are typically delivered 12-24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 3 in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: 1 Gb/production, 4 G/introduction, plus 512 Mb/256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2003 ITRS, the typical high-performance ASIC design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 70% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 63% at the production level, and less than 50–55% for smaller previous generation shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C=Af^2=0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=70% of total chip area, the $C_{AVE} = C/E = 0.37\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.37e-6 mm^2/bit = 397 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half the size of an SLC product cell size and will also have a "virtual area factor" that is half of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-node half-pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 16–25 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-node half-pitch

(f) units. Typically, the cell factor of the logic 4t gate is 2.5–3 times greater than an SRAM 6t cell area factor, and 40–80 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology node. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology node. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology node, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first 20K wafer-starts-per-month manufacturing facility.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.

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YIELD ENHANCEMENT

METROLOGY

MODELING