INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2006 UPDATE

LITHOGRAPHY

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LITHOGRAPHY

The following updates were made to the Lithography chapter for 2006:

DIFFICULT CHALLENGES

- Double exposure / patterning
  - Overlay of multiple exposures including mask image placement
  - Availability of software to split the pattern apply optical proximity correction (OPC), and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
  - Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
  - Photoresists with independent exposure of multiple passes
  - Fab logistics and process control to enable low cycle time impact that include on-time availability of additional reticles and efficient scheduling of multiple exposure passes

TECHNOLOGY REQUIREMENTS

- Mask tables
  - Color changes only: based on improvements in the industry
    - Optical mask tables, extreme ultra-violet lithography (EUVL) mask tables, and imprint template tables
  - Added lines for double exposure (mask image placement and mask critical dimension (CD) mean)
  - Corrected data volume values for EUVL
- Resist tables
  - Added lines for defects in double exposure processes
- Maskless lithography
  - Two lines added for grid size and data volume

POTENTIAL SOLUTIONS

- 45nm
  - 193i/H_2O
  - ADDED 193i double patterning
  - 193i with other fluids
  - EUV, maskless lithography (ML2)
- 32nm
  - EUV
  - ADDED 193i double patterning
  - 193i with other fluids and lens materials
  - ML2, Imprint
- 22/16nm
  - No dramatic changes
  - Changed order of ML2, Imprint

Table 74 Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography

MPU M1 contacted ½ pitch	*210 nm*	*160 nm*	*120 nm*	*90 nm*	*65 nm*	*45 nm*
k_1 Range [A]	*0.51–0.64*	*0.48–0.52*	*0.47–0.53*	*0.40–0.43*	*0.31–0.40*	*0.28–0.31*
Design rules	Minor restriction	Allow OPC and PSM, SRAF	Litho friendly design rules			
Restrictions (cumulative)	Minimum pitch, spacing and linewidth		Pitch and orientation	Contact locations, library cells checked for OPC compatibility and printability	Features on grid?, Restricted feature set?	
Masks (Optical proximity correction)	Rule-based OPC, MBOPC for gate, custom OPC for memory cells	Model-based OPC (MBOPC) on critical layers, SRAF on gate layer	Model-based OPC w /SRAF on critical layers, verification of entire corrected layout with simulation		Model-based OPC with vector simulation, SRAF, polarization corrections	Model-based OPC with vector simulation, SRAF, polarization corrections, variation of OPC intensity by location in circuit?, magnification increase?
(Gate and M1 layer mask type)		cPSM and EPSM		APSM, EPSM and hiT EPSM	APSM, hiT EPSM, dual dipole?	APSM, hiT EPSM, double exposure with 2× larger pitch
(Contacts/vias layers mask type)		EPSM		APSM, EPSM, HiT PSM		
Resist	Custom by layer type					
Thickness	<500 nm	<400 nm	<350 nm	<280 nm	<225 nm	<160 nm
Substrate	ARC	ARC, hard masks		ARC, hard masks, top coats		
Etch		Post development resist width reduction				
Tool		Selection based on aberrations, automated NA/sigma control		Aberration monitoring		
(Illumination)	Conventional, annular illumination	Off-axis illumination	Quadrupole	Custom illumination	Custom illumination, polarization optimization	Custom illumination, polarization optimization
(Dose control)		Cross wafer dose adjustments	Dose adjustment across the wafer and along scan			
(Process control (CD and overlay)	Offsets from previous lots	Automated process control with downloaded offsets			Automated process control with downloaded offsets, metrology integrated in lithography cell	

MBOPC—model based optical proximity correction cPSM—complementary PSM APSM—alternating PSM
EPSM—embedded PSM HiT—high transmission ARC—antireflection coating SRAF—sub-resolution assist features

Note for Table 74:
[A] Assumes that optical and immersion optical projection lithography is used.

DIFFICULT CHALLENGES

Table 75 Lithography Difficult Challenges UPDATED

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Optical masks with features for resolution enhancement and post-optical mask fabrication	Registration, CD, and defect control for masks
	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features
	Understanding polarization effects at the mask and effects of mask topography on imaging and optimizing mask structures to compensate for these effects
	Eliminating formation of progressive defects and haze during exposure
	Determining optimal mask magnification ratio for <45 nm half pitch patterning with 193 nm radiation and developing methods, such as stitching, to compensate for the potential use of smaller exposure fields
	Development of defect free 1× templates
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time
	Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume
	Sufficient lifetime for exposure tool technologies
	Resources for developing multiple technologies at the same time
	ROI for small volume products
	Stages, overlay systems and resist coating equipment development for wafers with 450 mm diameter
Process control	Processes to control gate CDs to < 4 nm 3σ
	New and improved alignment and overlay control methods independent of technology option to <11 nm 3σ overlay error
	Controlling LER, CD changes induced by metrology, and defects < 50 nm in size
	Greater accuracy of resist simulation models
	Accuracy of OPC and OPC verification, especially in presence of polarization effects
	Control of and correction for flare in exposure tool, especially for EUV lithography
	Lithography friendly design and design for manufacturing (DFM)
Immersion lithography	Control of defects caused in immersion environment, including bubbles and staining
	Resist chemistry compatibility with fluid or topcoat and development of topcoats
	Resists with index of refraction > 1.8
	Fluid with refractive index > 1.65 meeting viscosity, absorption, and fluid recycling requirements
	Lens materials with refractive index >1.65 meeting absorption and birefringence requirements for lens designs

Table 75 Lithography Difficult Challenges (continued) UPDATED

	Difficult Challenges ≥ 32 nm	*Summary of Issues*
	EUV lithography	Low defect mask blanks, including defect inspection with < 30 nm sensitivity and blank repair
		Source power > 115 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components
		Resist with < 3 nm 3σ LWR, < 10 mJ/cm^2 sensitivity and < 40 nm ½ pitch resolution
		Fabrication of optics with < 0.10 nm rms figure error and < 10% intrinsic flare
		Controlling optics contamination to achieve > five-year lifetime
		Protection of masks from defects without pellicles
		Mix and match with optical lithography
ADD	**Double patterning**	**Overlay of multiple exposures including mask image placement**
		Availability of software to split the pattern apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
		Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
		Photoresists with independent exposure of multiple passes
		Fab logistics and process control to enable low cycle time impact that include on-time availability of additional reticles and efficient scheduling of multiple exposure passes
	Difficult Challenges < 32 nm	*Summary of Issues*
	Mask fabrication	Defect-free masks, especially for 1× masks for imprint and EUVL mask blanks free of printable defects
		Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair), especially for 1× masks
		Mask process control methods and yield enhancement
		Protection of EUV masks and imprint templates from defects without pellicles
		Phase shifting masks for EUV
	Metrology and defect inspection	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3σ
		Metrology for achieving < 2.8 nm 3σ overlay error
		Defect inspection on patterned wafers for defects < 30 nm, especially for maskless lithography
		Die-to-database inspection of wafer patterns written with maskless lithography
	Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
		Development of cost-effective optical and post-optical masks
		Achieving ROI for industry with sufficient lifetimes for exposure tool technologies and ROI for small volume products
	Gate CD control improvements and process control	Development of processes to control gate CD < 1.3 nm 3σ with < 1.5 nm 3σ line width roughness
		Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3σ overlay error, especially for imprint lithography
		Process control and design for low k_1 optical lithography
	Resist materials	Resist and antireflection coating materials composed of alternatives to PFAS compounds
		Limits of chemically amplified resist sensitivity for < 32 nm half pitch due to acid diffusion length
		Materials with improved dimensional and LWR control

TECHNOLOGY REQUIREMENTS

Table 76a Lithography Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
DRAM and Flash									
DRAM ½ pitch (nm)	80	70	65	57	50	45	40	35	32
Flash ½ pitch (nm) (un-contacted poly)	76	64	57	51	45	40	36	32	28
Contact in resist (nm)	94	79	70	63	56	50	44	39	35
Contact after etch (nm)	85	72	64	57	51	45	40	36	32
Overlay [A] (3 sigma) (nm)	◆15	◆13	◆11	10	9	8	7.1	6.4	5.7
CD control (3 sigma) (nm) [B]	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
MPU									
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32
MPU gate in resist (nm)	54	48	42	38	34	30	27	24	21
*MPU physical gate length (nm) **	32	28	25	23	20	18	16	14	13
Contact in resist (nm)	111	97	84	73	64	56	50	44	39
Contact after etch (nm)	101	88	77	67	58	51	45	40	36
*Gate CD control (3 sigma) (nm) [B] ***	◆3.3	◆2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32
Chip size (mm^2)									
Maximum exposure field height (mm)	26	26	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858	858	858
Number of mask levels MPU	33	33	33	35	35	35	35	35	35
Number of mask levels DRAM	24	24	24	24	24	26	26	26	26
Wafer size (diameter, mm)	300	300	300	300	300	300	300	450	450

** MPU physical gate length numbers and colors are determined by several working groups and the ORTC.*
*** Noted exception for RED in next three years: Solution NOT known, but does not prevent production manufacturing.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

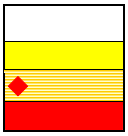
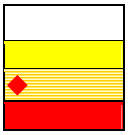


Table 76b Lithography Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
DRAM and Flash							
DRAM ½ pitch (nm)	28	25	22	20	18	16	14
Flash ½ pitch (nm) (un-contacted poly)	25	23	20	18	16	14	13
Contact in resist (nm)	31	28	25	22	20	18	16
Contact after etch (nm)	28	25	23	20	18	16	14
Overlay [A] (3 sigma) (nm)	5.1	4.5	4.0	3.6	3.2	2.8	2.5
CD control (3 sigma) (nm) [B]	3.0	2.6	2.3	2.1	1.9	1.7	1.5
MPU							
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	28	25	23	20	18	16	14
MPU gate in resist (nm)	19	17	15	13	12	11	9
*MPU physical gate length (nm) **	11	10	9	8	7	6	6
Contact in resist (nm)	35	31	28	25	22	20	18
Contact after etch (nm)	32	28	25	23	20	18	16
Gate CD control (3 sigma) (nm) [B]	1.2	1.0	0.9	0.8	0.7	0.7	0.6
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	28	25	23	20	18	16	14
Chip size (mm^2)							
Maximum exposure field height (mm)	26	26	26	26	26	26	26
Maximum exposure field length (mm)	33	33	33	33	33	33	33
Maximum field area printed by exposure tool (mm^2)	858	858	858	858	858	858	858
Number of mask levels MPU	37	37	39	39	39	39	39
Number of mask levels DRAM	26	26	26	26	26	26	26
Wafer size (diameter, mm)	450	450	450	450	450	450	450

** MPU physical gate length numbers and colors are determined by several working groups and the ORTC.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 76a and b:
[A] Overlay (nm)—Overlay is a vector component (in X and Y directions) quantity defined at every point on the wafer. It is the difference, O, between the vector position, P1, of a substrate geometry, and the vector position of the corresponding point, P2, in an overlaying pattern, which may consist of resist. O=P1-P2. The difference, O, is expressed in terms of vector components in the X and Y directions, and the value shown is three times the standard deviation of overlay values on the wafer.
[B] CD control (nm)—Control of critical dimensions compared to mean linewidth target at all pattern pitch values, including errors from all lithographic sources (due to masks, imperfect optical proximity correction, exposure tools, and resist) at all spatial length scales (e.g., includes errors across exposure field, across wafer, between wafers and between wafer lots)

Table 77a Resist Requirements—Near-term Years UPDATED

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
Flash ½ pitch (nm) (un-contacted poly)	*76*	*64*	*57*	*51*	*45*	*40*	*36*	*32*	*28*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU physical gate length (nm) [after etch]	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
MPU gate in resist length (nm)	**53**	**47**	**42**	**38**	**33**	**30**	**27**	**24**	**21**
*Resist Characteristics **									
*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) **†*	◆3.3	◆2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
*Resist thickness (nm, single layer) ****	150-265	125-225	110-200	100-180	90-160	80-145	70-130	60-115	55-100
PEB temperature sensitivity (nm/C)	2	1.75	1.75	1.5	1.5	1.5	1.5	1.5	1
Backside particle density (particles/cm^2)	0.57	0.57	0.28	0.28	0.28	0.28	0.28	0.28	0.28
Back surface particle diameter: lithography and measurement tools (nm)	160	120	120	120	100	100	100	100	75
Defects in spin-coated resist films (#/cm^2) †	◆0.01	◆0.01	◆0.01	0.01	0.01	0.01	0.01	0.01	0.01
Minimum defect size in spin-coated resist films (nm)	◆50	◆45	◆40	35	30	30	20	20	20
Defects in patterned resist films, gates, contacts, etc. (#/cm^2)	◆0.05	◆0.04	◆0.04	0.03	0.03	0.03	0.02	0.02	0.02
Minimum defect size in patterned resist (nm)	◆50	◆45	◆40	35	30	30	20	20	20
*Low frequency line width roughness: (nm, 3 sigma) <8% of CD ******	4.2	3.8	3.4	3	2.7	2.4	2.1	1.9	1.7
ADD *Defects in spin-coated resist films for double patterning (#/cm2)*	0.005	0.005	0.005	0.005	0.005	0.005	0.005	0.005	0.005
ADD *Backside particle density for double patterning (#/cm2)*	0.285	0.285	0.14	0.14	0.14	0.14	0.14	0.14	0.14

† *Noted exception for RED in next three years: Solution NOT known, but does not prevent production manufacturing.*

Table 77b Resist Requirements—Long-term Years UPDATED

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Flash ½ pitch (nm) (un-contacted poly)	*25*	*23*	*20*	*18*	*16*	*14*	*13*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU physical gate length (nm) [after etch]	*11*	*10*	*9*	*8*	*7*	*6*	*6*
MPU gate in resist length (nm)	**19**	**17**	**15**	**13**	**12**	**11**	**9**
*Resist Characteristics **							
*Resist meets requirements for gate resolution and gate CD control (nm, 3 sigma) **†*	1.2	1	0.9	0.8	0.7	0.7	0.6
*Resist thickness (nm, single layer) ****	50-90	45-80	40-75	35-65	30-60	25-50	25-45
PEB temperature sensitivity (nm/C)	1	1	1	1	1	11	11
Backside particle density (particles/cm^2)	0.28	0.28	0.28	0.28	0.28	0.28	0.28
Back surface particle diameter: lithography and measurement tools (nm)	75	75	50	50	50	50	50
Defects in spin-coated resist films (#/cm^2)	0.01	0.01	0.01	0.01	0.01	0.01	0.01
Minimum defect size in spin-coated resist films (nm)	20	10	10	10	10	10	10
Defects in patterned resist films, gates, contacts, etc. (#/cm^2)	0.02	0.01	0.01	0.01	0.01	0.01	0.01
Minimum defect size in patterned resist (nm)	20	10	10	10	10	10	10
*Low frequency line width roughness: (nm, 3 sigma) <8% of CD ******	1.5	1.3	1.2	1.1	0.9	0.8	0.8
ADD *Defects in spin-coated resist films for double patterning (#/cm2)*	0.005	0.005	0.005	0.005	0.005	0.005	0.005
ADD *Backside particle density for double patterning (#/cm2)*	0.14	0.14	0.14	0.14	0.14	0.14	0.14

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known ◆
Manufacturable solutions are NOT known

Notes for Table 77a and b:
Exposure Dependent Requirements
** Resist sensitivity is treated separately in the second resist sensitivity table.*
*** Indicates whether the resist has sufficient resolution, CD control, and profile to meet the resolution and gate CD control values.*
**** Resist thickness is determined by the aspect ratio range of 2.0:1 to 3.5:1, limited by pattern collapse.*
***** Linked with resolution.*
****** LWR_{Lf} is 3σ deviation of spatial frequencies from 0.5 μm^{-1} to 1/(2*MPU ½ Pitch).*
Note: Standard deviation is determined by biased estimate (corrected for SEM noise) of linewidth variation over a greater than or equal 2 µm measured at less than or equal 4 nm intervals.
† Defects in coated films are those detectable as physical objects, such as pinholes, that may be distinguished from the resist film by optical detection methods.
Other requirements:
[A] Need for a positive tone resist and a negative tone resist will depend upon critical feature type and density.
[B] Feature wall profile should be 90 ± 2 degrees.
{C] Thermal stability should be ≥ 130 ℃.
[D] Etching selectivity should be > that of poly hydroxystyrene (PHOST).
[E] Upon removal by stripping there should be no detectible residues.
[F] Sensitive to basic airborne compounds such as amines and amides. Clean handling space should have < 1000 pptM of these materials.
[G] Metal contaminants < 5 ppb.
[H] Organic material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 193 nm lithography tool is < 1e12. Value for EUV lithography tool is < 5e13. Values for electron beam are being determined.
[I] Si containing material outgassing (molecules/cm^2-sec) for two minutes (under the lens). Value for 193 nm lithography tool is < 1e8. Value for EUV lithography tool is < 5e13. Values for electron beam are being determined.

Table 77c Resist Sensitivities

Exposure Technology	*Sensitivity*
248 nm	**10–50 mJ/ cm^2**
193 nm	**20–50 mJ/ cm^2**
Extreme Ultraviolet at 13.5 nm	**5–15 mJ/ cm^2**
High Voltage Electron Beam (50–100 kV) ********	**5–10 µC/ cm^2**
Low Voltage Electron Beam (1–2 kV) ********	**0.2–1.0 µC/ cm^2**

***** Linked with resolution*

Notes for Table 77c
Due to shot noise effects, the required sensitivity will increase with decreasing critical feature size. Sensitivity may increase beyond the table values for 22nm half-pitch and smaller dimensions.

Table 78a Optical Mask Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	DRAM/Flash CD control (3 sigma) (nm)	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
	MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU gate in resist (nm)	54	48	42	38	34	30	27	24	21
	MPU physical gate length (nm)	32	28	25	23	20	18	16	14	13
ADD	Gate CD control (3 sigma) (nm) [A]	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
	Overlay (3 sigma) (nm)	15	13	11	10	9	8	7	6	6
	Contact after etch (nm)	85	72	64	57	51	45	40	36	32
	Mask magnification [B]	4	4	4	4	4	4	4	4	4
WAS	Mask nominal image size (nm) [C]	214	191	170	151	135	120	107	95	85
IS	Mask nominal image size (nm) [C]	214	191	170	151	135	120	107	95	85
WAS	Mask minimum primary feature size [D]	150	133	◆119	106	94	84	75	67	59
IS	Mask minimum primary feature size [D]	150	133	119	106	94	84	75	67	59
WAS	Mask sub-resolution feature size (nm) opaque [E]	◆107	◆95	◆85	76	67	60	54	48	42
IS	Mask sub-resolution feature size (nm) opaque [E]	107	95	85	76	67	60	54	48	42
WAS	Image placement (nm, multipoint) [F]	◆9	◆8	◆7	6.1	5.4	4.8	4.3	3.8	3.4
IS	Image placement (nm, multipoint) [F]	9	8	7	6.1	5.4	4.8	4.3	3.8	3.4
	CD uniformity allocation to mask (assumption)	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
	MEEF isolated lines, binary or attenuated phase shift mask [G]	1.4	1.4	1.6	1.8	2	2.2	2.2	2.2	2.2
WAS	CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H] *	◆3.8	◆3.4	2.6	2.1	1.7	1.3	1.2	1.1	1
IS	CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H] *	3.8	3.4	2.6	2.1	1.7	1.3	1.2	1.1	1
WAS	MEEF dense lines, binary or attenuated phase shift mask [G]	2	2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
IS	MEEF dense lines, binary or attenuated phase shift mask [G]	2	2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
WAS	CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	7.1	6	4.8	4.3	3.8	3.4	3	2.7	2.4
IS	CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	7.1	6	4.8	4.3	3.8	3.4	3	2.7	2.4
WAS	MEEF contacts [G]	3	3	3.5	4	4	4	4	4	4
IS	MEEF contacts [G]	3	3	3.5	4	4	4	4	4	4
WAS	CD uniformity (nm, 3 sigma), contact/vias [K] *	◆4.7	◆4	3	2.4	2.1	1.9	1.7	1.5	1.3
IS	CD uniformity (nm, 3 sigma), contact/vias [K] *	4.7	4	3	2.4	2.1	1.9	1.7	1.5	1.3
WAS	Linearity (nm) [L]	13	11	10	9	8	7.2	6.4	5.6	5.1
IS	Linearity (nm) [L]	13	11	10	9	8	7.2	6.4	5.6	5.1
	CD mean to target (nm) [M]	6.4	5.6	5.2	4.6	4	3.6	3.2	2.8	2.6
WAS	Defect size (nm) [N] *	◆64	◆56	◆52	46	40	36	32	28	26
IS	Defect size (nm) [N] *	64	56	52	46	40	36	32	28	26
WAS	Blank flatness (nm, peak-valley) [O]	500	500	250	250	250	175	175	175	150
IS	Blank flatness (nm, peak-valley) [O]	500	500	250	250	250	175	175	175	150
	Data volume (GB) [P]	260	328	413	520	655	825	1040	1310	1651
	Mask design grid (nm) [Q]	4	2	2	2	2	2	2	2	2
	Attenuated PSM transmission mean deviation from target (± % of target) [R]	5	4	4	4	4	4	4	4	4
	Attenuated PSM transmission uniformity (±% of target) [R]	4	4	4	4	4	4	4	4	4
	Attenuated PSM phase mean deviation from 180° (± degree) [S]	3	3	3	3	3	3	3	3	3
WAS	Alternating PSM phase mean deviation from nominal phase angle target (± degree) [S]	◆2	1.5	1.5	1	1	1	1	1	1
IS	Alternating PSM phase mean deviation from nominal phase angle target (± degree) [S]	2	◆1.5	◆1.5	1	1	1	1	1	1
	Alternating PSM phase uniformity (± degree) [T]	◆2	◆1	◆1	1	1	1	1	1	1
ADD	Image placement (nm, multipoint) for double patterning	6.4	5.7	4.9	4.3	3.8	3.4	3.0	2.7	2.4
ADD	Difference in CD Mean-to-target for two masks used as a double patterning set (nm) [U]	◆3.2	◆2.8	◆2.6	◆2.3	2	1.8	1.6	1.4	1.3
	Mask materials and substrates	Absorber/attenuator on fused silica								
		Pellicle for optical masks for exposure wavelengths down to 193 nm, including masks for 193 nm immersion.								

Table 78b Optical Mask Requirements—Long-term Years UPDATED

					Optical masks not part of potential solutions. beyond 22 nm			
	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	DRAM/Flash CD control (3 sigma) (nm)	*3*	*2.6*	*2.3*	*2.1*	*1.9*	*1.7*	*1.5*
	MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU gate in resist (nm)	*19*	*17*	*15*	*13*	*12*	*11*	*9*
	MPU physical gate length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
ADD	*Gate CD control (3 sigma) (nm) [A]*	*1.2*	*1*	*0.9*	*0.8*	*0.7*	*0.7*	*0.6*
	Overlay (3 sigma) (nm)	*5*	*5*	*4*	*4*	*3*	*3*	*3*
	Contact after etch (nm)	*28*	*25*	*23*	*20*	*18*	*16*	*14*
	Mask magnification [B]	4	4	4	4	4	4	4
	Mask nominal image size (nm) [C]	76	67	60	54	48	42	38
	Mask minimum primary feature size [D]	53	47	42	37	33	30	26
	Mask sub-resolution feature size (nm) opaque [E]	38	34	30	27	24	21	19
	Image placement (nm, multipoint) [F]	2.7	2.4	2.2	1.9	1.7	1.5	1.4
	CD uniformity allocation to mask (assumption)	0.4	0.4	0.4	0.4	0.4	0.4	0.4
	MEEF isolated lines, binary or attenuated phase shift mask [G]	2.2	2.2	2.2	2.2	2.2	2.2	2.2
	CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	0.9	0.8	0.7	0.6	0.5	0.5	0.4
WAS	*MEEF dense lines, binary or attenuated phase shift mask [G]*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
IS	*MEEF dense lines, binary or attenuated phase shift mask [G]*	2.2	2.2	2.2	2.2	2.2	2.2	2.2
	CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	2.1	1.9	1.7	1.5	1.4	1.2	1.1
WAS	*MEEF contacts [G]*	4	4	4	4	4	4	4
IS	*MEEF contacts [G]*	4	4	4	4	4	4	4
	CD uniformity (nm, 3 sigma), contact/vias [K]	1.2	1.1	0.9	0.8	0.7	0.7	0.6
	Linearity (nm) [L]	4.5	4	3.5	3.2	2.9	2.6	2.2
	CD mean to target (nm) [M]	2.2	2	1.8	1.6	1.4	1.3	1.1
	*Defect size (nm) [N] **	22	20	18	16	14	13	11
WAS	*Blank flatness (nm, peak-valley) [O]*	150	150	125	125	125	100	100
IS	*Blank flatness (nm, peak-valley) [O]*	150	150	125	125	125	◆100	◆100
	Data volume (GB) [P]	2080	2621	3302	4160	5241	6604	8320
	Mask design grid (nm) [Q]	2	2	2	1	1	1	1
	Attenuated PSM transmission mean deviation from target (± % of target) [R]	4	4	4	4	4	4	4
	Attenuated PSM transmission uniformity (±% of target) [R]	4	4	4	4	4	4	4
	Attenuated PSM phase mean deviation from 180° (± degree) [S]	3	3	3	3	3	3	3
	Alternating PSM phase mean deviation from nominal phase angle target (± degree) [S]	1	1	1	1	1	1	1
	Alternating PSM phase uniformity (± degree) [T]	1	1	1	1	1	1	1
ADD	*Image placement (nm, multipoint) for double patterning*	1.9	1.7	1.6	1.3	1.2	1.1	1.0
ADD	*Difference in CD Mean-to-target for two masks used as a double patterning set (nm) [U]*	1.1	1	0.9	0.8	0.7	0.65	0.55
	Mask materials and substrates	Absorber/attenuator on fused silica						
		Pellicle for optical masks for exposure wavelengths down to 193 nm, including masks for 193 nm immersion.						

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known ◆

Manufacturable solutions are NOT known

Notes for Table 78a and b:

ADD ***[A] Gate CD Control (nm)—Control of critical dimensions at the mask compared to mean line width target at all pattern pitch values for the gate level.***

[B] Magnification—Lithography tool reduction ratio.

[C] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio.

[D] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD placement and defects.

[E] Mask Sub-Resolution Feature Size—The minimum width of non-printing features on the mask such as sub-resolution assist features.

[F] Image Placement—The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error. These values do not comprehend additional image placement error induced by pellicle mount and mask clamping in the exposure tool.

[G] The CD error on the wafer is directly proportional to the CD error on the mask where mask error enhancement factor (MEEF) is the constant of proportionality. An MEEF value greater than unity therefore imposes a more stringent CD uniformity requirement on the mask to maintain the CD uniformity budget on the wafer.

[H] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and isolated features on a binary mask.

[I] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitch features on a quartz shifter phase mask.

[J] CD Uniformity—The three-sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitch features on a binary or attenuated phase shift mask.

[K] CD Uniformity—The three-sigma deviation of square root of contact area on a mask through multiple pitches.

[L] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are equal to the smallest sub-resolution assist mask feature and up to three times the minimum wafer half pitch multiplied by the magnification.

[M] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed to feature size (design size). Applies to a single feature size and tone. Σ(Actual-Target)/Number of measurements.

[N] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation. Printable 180-degree phase defects are 70% smaller than the number shown.

[O] Blank Flatness—Flatness is nanometers, peak-to-valley across the 140 mm × 140 mm central area image field on a 6-inch × 6-inch square mask blank. Flatness is derived from wafer lithography DOF requirements for each printing the desired feature dimensions.

[P] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a pattern generator tool.

[Q] Mask Design Grid—Wafer design grid multiplied by the mask magnification.

[R] Transmission—Ratio, expressed in percent, of the fraction of light passing through an attenuated PSM layer relative to the mask blank with no opaque films.

[S] Phase—Change in optical path length between two regions on the mask expressed in degrees. The mean value is determined by averaging phase measured for many features on the mask.

[T] Alt PSM phase uniformity is a range specification equal to the maximum phase error deviation of any point from the mean value.

[U] Difference in CD mean-to-target for two masks refers to the mask CD of each of the masks that makes up the matched set of two masks used to form a single circuit level in double patterning.

Table 78c EUVL Mask Requirements—Near-term Years UPDATED

	Year of Production	2008	2009	2010	2011	2012	2013
	DRAM ½ pitch (nm) (contacted)	57	50	45	40	36	32
	Flash ½ pitch (nm) (un-contacted poly)	51	45	40	36	32	28
	DRAM/Flash CD control (3 sigma) (nm)	5.9	5.3	4.7	4.2	3.7	3.3
	MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	59	52	45	40	36	32
	MPU gate in resist (nm)	38	34	30	27	24	21
	MPU physical gate length (nm)	23	20	18	16	14	13
ADD	Gate CD control (3 sigma) (nm) [A]	2.3	2.1	1.9	1.7	1.5	1.3
	Overlay	10	9	8	7	6	6
	Contact after etch (nm)	57	51	45	40	36	32
	Generic Mask Requirements						
	Mask magnification [B]	4	4	4	4	4	4
WAS	Mask nominal image size (nm) [C]	151	135	120	107	95	85
IS	Mask nominal image size (nm) [C]	151	135	120	107	95	85
WAS	Mask minimum primary feature size [D]	106	94	84	75	67	59
IS	Mask minimum primary feature size [D]	106	94	84	75	67	59
WAS	Image placement (nm, multipoint) [E]	6.1	5.4	4.8	4.3	3.8	3.4
IS	Image placement (nm, multipoint) [E]	6.1	5.4	4.8	4.3	3.8	3.4
	CD uniformity (nm, 3 sigma) [F]						
WAS	Isolated lines (MPU gates)	3.4	3	2.7	2.4	2.1	1.9
IS	Isolated lines (MPU gates)	3.4	3	2.7	2.4	2.1	1.9
WAS	Dense lines DRAM (half pitch)	8.2	7.3	6.5	5.8	5.2	4.6
IS	Dense lines DRAM (half pitch)	8.2	7.3	6.5	5.8	5.2	4.6
WAS	Contact/vias	7.6	6.8	4.8	4.3	3.8	3.4
IS	Contact/vias	7.6	6.8	4.8	4.3	3.8	3.4
WAS	Linearity (nm) [G]	8.7	7.6	6.8	6.1	5.3	4.9
IS	Linearity (nm) [G]	8.7	7.6	6.8	6.1	5.3	4.9
	CD mean to target (nm) [H]	4.6	4	3.6	3.2	2.8	2.6
	Defect size (nm) [I]	46	40	36	32	28	26
WAS	Data volume (GB) [J]	655	825	1040	1310	1651	2080
IS	Data volume (GB) [J]	413	520	655	825	1040	1310
	Mask design grid (nm) [K]	2	2	2	2	2	2
	EUVL-specific Mask Requirements						
	Substrate defect size (nm) [L]	38	36	35	33	31	30
	Mean peak reflectivity	65%	66%	66%	66%	67%	67%
	Peak reflectivity uniformity (% 3 sigma absolute)	0.69%	0.58%	0.47%	0.42%	0.37%	0.33%
	Reflected centroid wavelength uniformity (nm 3 sigma) [M]	0.08	0.07	0.06	0.05	0.05	0.05
	Absorber sidewall angle tolerance (± degrees) [P]	1	1	0.75	0.69	0.62	0.5
	Absorber LER (3 sigma nm) [N]	3.2	2.8	2.5	2.2	2	1.8
	Mask substrate flatness (nm peak-to-valley) [O]	75	60	50	41	36	32

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

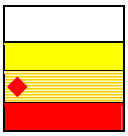
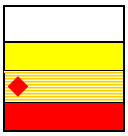


Table 78d EUVL Mask Requirements—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ pitch (nm) (contacted)	28	25	22	20	18	16	14
	Flash ½ pitch (nm) (un-contacted poly)	25	23	20	18	16	14	13
	DRAM/Flash CD control (3 sigma) (nm)	3	2.6	2.3	2.1	1.9	1.7	1.5
	MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	28	25	22	20	18	16	14
	MPU gate in resist (nm)	19	17	15	13	12	11	9
	MPU physical gate length (nm)	11	10	9	8	7	6	6
ADD	Gate CD control (3 sigma) (nm) [A]	1.2	1	0.9	0.8	0.7	0.7	0.6
	Overlay	5	5	4	4	3	3	3
	Contact after etch (nm)	28	25	23	20	18	16	14
	Generic Mask Requirements							
	Mask magnification [B]	4	4	4	4	4	4	4
	Mask nominal image size (nm) [C]	76	67	60	54	48	42	38
	Mask minimum primary feature size [D]	53	47	42	37	33	30	26
	Image placement (nm, multipoint) [E]	3	2.7	2.4	2.1	1.9	1.7	1.5
	CD Uniformity (nm, 3 sigma) [F]							
	Isolated lines (MPU gates)	1.7	1.5	1.3	1.2	1.1	1	0.9
WAS	Dense lines DRAM (half pitch)	4.1	3.7	3.3	2.9	2.6	2.3	2.1
IS	Dense lines DRAM (half pitch)	4.1	3.7	3.3	2.9	2.6	2.3	2.1
	Contact/vias	3	2.7	1.8	1.6	1.4	1.3	1.1
	Linearity (nm) [G]	4.3	3.8	3.3	3	2.7	2.4	2.1
	CD mean to target (nm) [H]	2.2	2	1.8	1.6	1.4	1.3	1.1
	Defect size (nm) [I]	22	20	18	16	14	13	11
WAS	Data volume (GB) [J]	2621	3302	4160	5241	6604	8320	10483
IS	Data volume (GB) [J]	1651	2080	2621	3302	4160	5241	6604
	Mask design grid (nm) [K]	2	2	2	1	1	1	1
	EUVL-specific Mask Requirements							
	Substrate defect size (nm) [L]	28	27	25	23	22	20	18
	Mean peak reflectivity	67%	67%	67%	67%	67%	67%	67%
	Peak reflectivity uniformity (% 3 sigma absolute)	0.29%	0.26%	0.23%	0.21%	0.19%	0.17%	0.15%
	Reflected centroid wavelength uniformity (nm 3 sigma) [M]	0.04	0.04	0.04	0.03	0.03	0.03	0.02
	Absorber sidewall angle tolerance (± degrees) [P]	0.5	0.5	0.5	0.5	0.5	0.5	0.5
	Absorber LER (3 sigma nm) [N]	1.6	1.4	1.3	1.1	1	0.9	0.8
	Mask substrate flatness (nm peak-to-valley) [O]	29	26	23	20	18	16	14

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 78c and d:
EUVL masks are patterned absorber layers on top of multilayers that are deposited on low thermal expansion material substrates.

ADD *[A] Gate CD Control (nm)—Control of critical dimensions at the mask compared to mean line width target at all pattern pitch values for the gate level.*

[B] Magnification—Lithography tool reduction ratio.
[C] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio.
[D] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD, placement, and defects.
[E] Image Placement—The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error.
[F] CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the mask feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt (Area)—sqrt (Target Area).
[G] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than the mask minimum primary feature size and up to three times the minimum wafer half pitch multiplied by the magnification.
[H] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed-to feature size (design size). Applies to a single feature size and tone. Σ(Actual-Target)/Number of measurements.
[I] Defect Size—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.

[J] Data Volume—This is the expected maximum file size for uncompressed data for a single layer as presented to a pattern generator tool.
[K] Mask Design Grid—Wafer design grid multiplied by the mask magnification.
[L] Substrate Defect Size—the minimum diameter spherical defect (in polystyrene latex sphere equivalent dimensions) on the substrate beneath the multilayers that causes an unacceptable linewidth change in the printed image. Substrate defects might cause phase errors in the printed image and are the smallest mask blank defects that would unacceptably change the printed image.
[M] Includes variation in median wavelength over the mask area and mismatching of the average wavelength to the wavelength of the exposure tool optics.
[N] Line edge roughness (LER)—is defined a roughness 3 sigma one-sided for spatial period <mask primary feature size.
[O] Mask Substrate Flatness—Residual flatness error (nm peak-to-valley) over the mask excluding a 5 mm edge region on all sides after removing wedge, which may be compensated by the mask mounting and leveling method in the exposure tool. The flatness error is defined as the deviation of the surface from the plane that minimizes the maximum deviation. This flatness requirement applies to each of the front and backsides individually.
[P] The sidewall angle tolerance applies to the mean absorber sidewall angle agreed upon between mask user and supplier.

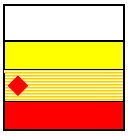
Table 78e Imprint Template Requirements—Near-term Years UPDATED

	Year of Production	2008	2009	2010	2011	2012	2013
	DRAM ½ pitch (nm) (contacted)	57	50	45	40	36	32
	Flash ½ pitch (nm) (un-contacted poly)	51	45	40	36	32	28
	DRAM/Flash CD control (3 sigma) (nm)	5.9	5.3	4.7	4.2	3.7	3.3
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	59	52	45	40	36	32
	MPU gate in resist (nm)	38	34	30	27	24	21
	MPU physical gate length (nm)	23	20	18	16	14	13
	Overlay (3 sigma) (nm)	5.9	5.3	4.7	4.2	3.7	3.3
ADD	Gate CD control (3 sigma) (nm)[A]	2.3	2.1	1.9	1.7	1.5	1.3
	Contact after etch (nm)	67	58	51	45	40	36
	Generic Mask Requirements						
	Magnification [B]	1	1	1	1	1	1
	Mask nominal image size (nm) [C]	38	34	30	27	24	21
	Image placement (nm, multipoint) [D]	2	1.8	1.6	1.4	1.2	1.1
	CD Uniformity (nm, 3 sigma) [E]						
	Isolated lines (MPU gates)	2.2	1.9	1.7	1.5	1.4	1.2
WAS	Dense lines DRAM/Flash (half pitch)	5.5	4.9	4.3	3.9	3.4	3.1
IS	Dense lines DRAM/Flash (half pitch)	5.5	4.9	4.3	3.9	3.4	3.1
WAS	Contact/vias	6.4	5.6	4.9	4.3	3.9	3.4
IS	Contact/vias	6.4	5.6	4.9	4.3	3.9	3.4
WAS	Linearity (nm) [F]	5.1	4.5	4	3.6	3.2	2.8
IS	Linearity (nm) [F]	5.1	4.5	4	3.6	3.2	2.8
	CD mean to target (nm) [G]	5.1	4.5	4	3.6	3.2	2.8
	Data volume (GB) [H]	295	372	469	591	745	938
	Mask design grid (nm) [I]	1	1	1	1	1	1
	UV-NIL-specific Mask Requirements						
	Defect size impacting CD (nm) x, y [J]	5.1	4.5	4	3.6	3.2	2.8
	Defect size impacting CD (nm) z [K]	10.1	9	8	7.1	6.4	5.7
WAS	Mask substrate flatness (nm peak-to-valley) [L]	298	252	192	180	153	126
IS	Mask substrate flatness (nm peak-to-valley) [L]	298	252	192	180	153	126
	Trench depth, mean (nm) [M]	75–119	67–104	60–90	53–81	47–72	42–64
	Etch depth uniformity (nm) [N]	3.8–5.9	3.4–5.2	3.0–4.5	2.7–4.0	2.4–3.6	2.1–3.2
	Trench wall angle (degrees) [O]	87	87.3	87.6	87.9	88.1	88.3
	Trench width roughness (nm, 3 sigma) [P]	2.2	2	1.7	1.6	1.4	1.2
	Corner radius, bottom of feature (nm) [Q]	6.3	5.6	5	4.5	4	3.5
	Corner radius, top of feature (nm) [R]	1.6	1.4	1.3	1.1	1	0.9
	Trench bottom surface roughness (nm, 3 sigma) [S]	7.6	6.7	6	5.4	4.8	4.2
	Template absorption [T]	<2%	<2%	<2%	<2%	<2%	<2%
	Near surface defect (nm) [U]	51	45	40	36	32	28
WAS	Defect size, patterned template (nm) [V]	35	30	30	20	20	20
IS	Defect size, patterned template (nm) [V]	35	30	30	20	20	20
	Defect density (#/cm^2) [W]	0.03	0.03	0.03	0.01	0.01	0.01
	Dual Damascene overlay: metal/via (nm, 3 sigma) [X]	25	23	22	20	18	17

Table 78f Imprint Template Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Flash ½ pitch (nm) (un-contacted poly)	*25*	*23*	*20*	*18*	*16*	*14*	*13*
DRAM/Flash CD control (3 sigma) (nm)	*3.0*	*2.6*	*2.3*	*2.1*	*1.9*	*1.7*	*1.5*
MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU gate in resist (nm)	*19*	*17*	*15*	*13*	*12*	*11*	*9*
MPU physical gate length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Overlay (3 sigma) (nm)	*3.0*	*2.6*	*2.3*	*2.1*	*1.9*	*1.7*	*1.5*
*Gate CD control (3 sigma) (nm)**[A]*	*1.2*	*1.0*	*0.9*	*0.8*	*0.7*	*0.7*	*0.6*
Contact after etch (nm)	*32*	*28*	*25*	*23*	*20*	*18*	*16*
Generic Mask Requirements							
Magnification [B]	1	1	1	1	1	1	1
Mask nominal image size (nm) [C]	19	17	15	13	12	11	9
Image placement (nm, multipoint) [D]	1.0	0.9	0.8	0.7	0.6	0.6	0.5
CD Uniformity (nm, 3 sigma) [E]							
Isolated lines (MPU gates)	1.1	1.0	0.9	0.8	0.7	0.6	0.5
Dense lines DRAM/Flash (half pitch)	2.7	2.4	2.2	1.9	1.7	1.5	1.4
Contact/vias	3.1	2.7	2.4	2.2	1.9	1.7	1.5
Linearity (nm) [F]	2.5	2.3	2.0	1.8	1.6	1.4	1.3
CD mean to target (nm) [G]	2.5	2.3	2.0	1.8	1.6	1.4	1.3
Data volume (GB) [H]	1182	1489	1876	2364	2978	3752	4728
Mask design grid (nm) [I]	1	1	1	1	1	1	1
UV-NIL-specific Mask Requirements							
Defect size impacting CD (nm) x, y [J]	2.5	2.3	2.0	1.8	1.6	1.4	1.3
Defect size impacting CD (nm) z [K]	5.1	4.5	4.0	3.6	3.2	2.8	2.5
Mask substrate flatness (nm peak-to-valley) [L]	110	88	72	56	45	36	29
Trench depth, mean (nm) [M]	37–57	33–51	30–45	26–41	23–36	21–32	18–29
Etch depth uniformity (nm) [N]	1.9–2.8	1.7–2.5	1.5–2.3	1.3–2.0	1.2–1.8	1.1–1.6	0.9–1.4
Trench wall angle (degrees) [O]	88.5	88.7	88.8	88.9	89.1	89.2	89.2
Trench width roughness (nm, 3 sigma) [P]	1.1	1.0	0.9	0.8	0.7	0.6	0.5
Corner radius, bottom of feature (nm) [Q]	3.2	2.8	2.5	2.2	2.0	1.8	1.6
Corner radius, top of feature (nm) [R]	0.8	0.7	0.6	0.6	0.5	0.4	0.4
Trench bottom surface roughness (nm, 3 sigma) [S]	3.8	3.4	3.0	2.7	2.4	2.1	1.9
Template absorption [T]	<2%	<2%	<2%	<2%	<2%	<2%	<2%
Near surface defect (nm) [U]	25	23	20	18	16	14	13
Defect size, patterned template (nm) [V]	20	10	10	10	10	10	10
Defect density (#/cm^2) [W]	0.01	0.01	0.01	0.01	0.01	0.01	0.01
Dual Damascene overlay: metal/via (nm, 3 sigma) [X]	15	14	11	10.5	10	9	8

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 78e and f:

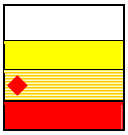
ADD *[A] Gate CD Control (nm)—Control of critical dimensions at the mask compared to mean line width target at all pattern pitch values for the gate level.*

[B] Magnification—Lithography tool reduction ratio, N:1.
[C] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio.
[D] The maximum component deviation (X or Y) of the array of the images centerline relative to a defined reference grid after removal of isotropic magnification error.
[E] CD Uniformity—The three sigma deviation of actual image sizes on a mask for a single size and tone critical feature. Applies to features in X and Y and multiple pitches from isolated to dense. Contacts: Measure and tolerance refer to the area of the mask feature. For table simplicity the roadmap numbers normalize back to one dimension. sqrt (Area)—sqrt (Target Area).
[F] Linearity—Maximum deviation between mask "Mean to Target" for a range of features of the same tone and different design sizes. This includes features that are greater than the mask minimum primary feature size and up to three times the minimum wafer half pitch multiplied by the magnification.
[G] CD Mean to Target—The maximum difference between the average of the measured feature sizes and the agreed-to feature size (design size). Applies to a single feature size and tone. S(Actual-Target)/Number of measurements.
[H] This is the expected maximum file size for uncompressed data for a single layer as presented to a raster write tool.
[I] Wafer design grid multiplied by the mask magnification.
[J] Defect Size (nm) x, y—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
[K] Defect Size (nm) z—A mask defect is any unintended mask anomaly that prints or changes a printed image size by 10% or more. The mask defect size listed in the roadmap are the square root of the area of the smallest opaque or clear "defect" that is expected to print for the stated generation.
[L] Flatness (nm peak-to-valley) across the 110 mm × 110 mm central area image field on a 6-inch × 6-inch square blank. Flatness is derived from empirical residual layer uniformity (RLT) and magnification.
[M] Trench depth mean—Aspect ratio of trench set to 2:1. Low end determined by printed gate length, High end determined by MPU/ASIC half pitch
[N] Trench depth uniformity in nm—Set to 5% of trench depth.
[O] Trench wall angle in degrees—Minimum wall angle necessary to keep the etch bias of the bilayer resist less than 5%. A selectivity of 10:1 between the etch barrier and transfer layer is assumed. Transfer layer aspect ratio starts at 1.5:1, and finishes at 2:1.
[P] Trench width roughness (nm, 3 sigma)—equivalent to resist line width roughness.
[Q] Corner radius, bottom of feature—critical to S-FIL/R (positive tone imprinting) where it defines the depth that the blanket ROI etch must reveal into the imprint material for good CD control (12.5% of CD). Non-critical for S-FIL (negative tone imprinting).
[R] Corner radius, top of feature—critical to S-FIL (negative tone imprinting) for good CD control, where it behaves as a resist "footing" in equivalent projection lithography (3% of CD). Non-critical for S-FIL/R (positive tone imprinting).
[S] Roughness in the bottom of an etched trenching resulting from imperfections in the plasma etch process or micromasking from the hard mask.
[T] Percent of incident light intrinsically absorbed by the 6.3 mm thick substrate at 365 nm. This is to minimize heating and thermal distortion and maximize equipment throughput.
[U] This is the maximum defect size for the quartz substrate from the surface level to a depth of 200 nm.
[V] Defect size, patterned template—Defect size in nm on finished patterned template.
[W] Number of defects per square cm on a finished template.
[X] This is the via to metal line overlay requirement on a 3D template for landed vias.

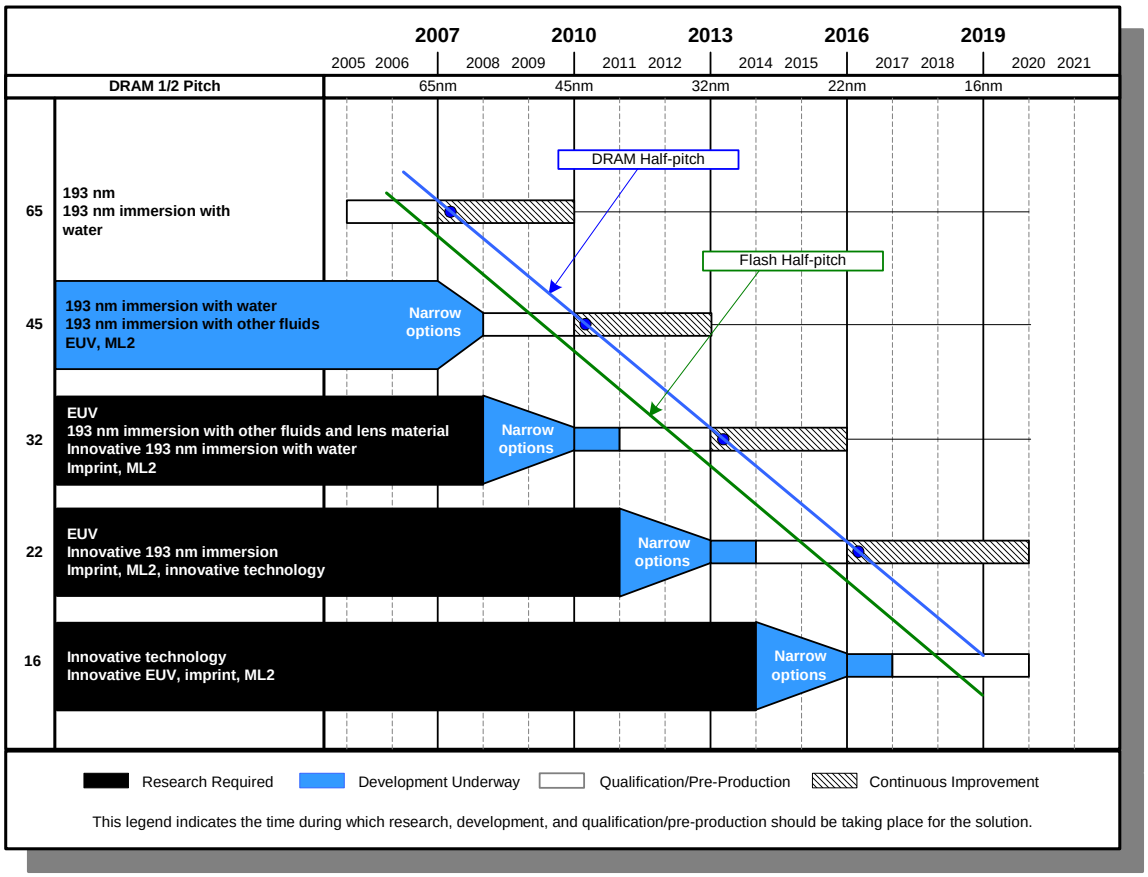
Table ML2 Maskless Lithography Technology Requirements ADDED

	Year of Production	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ pitch (nm) (contacted)	57	50	45	40	36	32	28	25	22	20	18	16	14
	DRAM/Flash CD control (3 sigma) (nm)	5.9	5.3	4.7	4.2	3.7	3.3	3	2.6	2.3	2.1	1.9	1.7	1.5
	MPU/ASIC Metal 1 (M1) ½ pitch (nm)(contacted)	59	52	45	40	36	32	28	25	22	20	18	16	14
	MPU gate in resist (nm)	38	34	30	27	24	21	19	17	15	13	12	11	9
	MPU physical gate length (nm)	23	20	18	16	14	13	11	10	9	8	7	6	6
	Gate CD control (3 sigma) (nm)	2.3	2.1	1.9	1.7	1.5	1.3	1.2	1	0.9	0.8	0.7	0.7	0.6
	Overlay (3 sigma) (nm)	10	9	8	7	6	6	5	5	4	4	3	3	3
	Contact after etch (nm)	57	51	45	40	36	32	28	25	23	20	18	16	14
ADD	Data Volume (GB)	655	825	1040	1310	1651	2080	2621	3302	4160	5241	6604	8320	10483
ADD	Grid Size (nm)	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.25	0.25	0.25	0.25

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

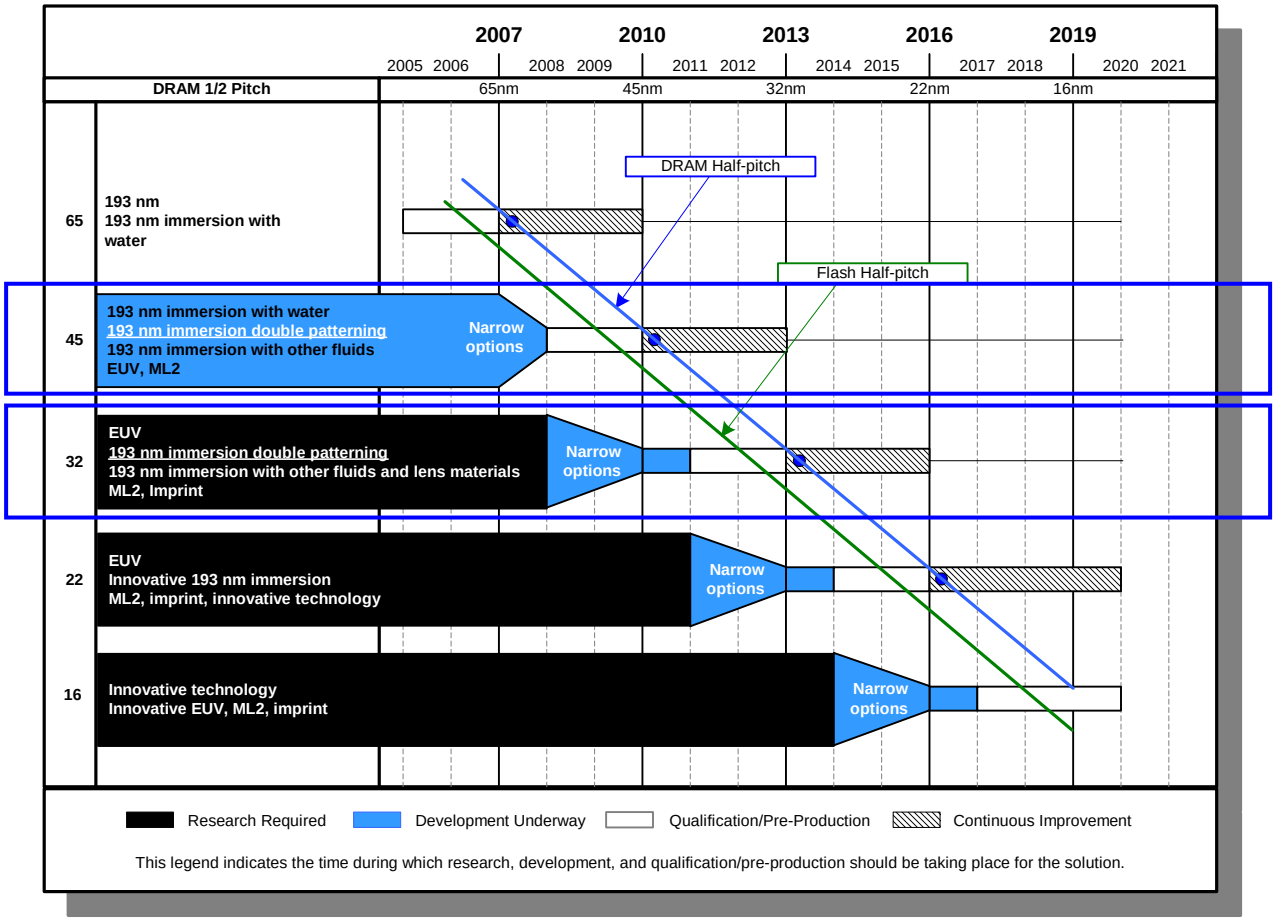


POTENTIAL SOLUTIONS



Notes: RET and lithography friendly design rules will be used with all optical lithography solutions, including with immersion; therefore, they are not explicitly noted.

Figure 67 Lithography Exposure Tool Potential Solutions - WAS



Notes: RET and lithography friendly design rules will be used with all optical lithography solutions, including with immersion; therefore, they are not explicitly noted.

*Figure 67 Lithography Exposure Tool Potential Solutions - **IS***