INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2006 UPDATE

METROLOGY

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METROLOGY

SUMMARY

During 2006, participation in the Metrology TWG increased. Supplier representation became more visible, and those members provided key insight for the group. Some of the changes initiated in 2006 will receive addition scrutiny in 2007, especially the impact of dual patterning on metrology. Changes in wafer level lithography metrology for CD were based on recent data showing in increased capability of CD metrology. Tightened tolerances for overlay indicate the need for acceleration of improvements in overlay metrology. In addition, the uncertainty associated with the timing of dual patterning combined with the lack of metrology for dual patterning a significant issue. Changes in the timing of the introduction of high κ and low κ change the timing of some metrology requirements.

Table 116 Metrology Difficult Challenges

Difficult Challenges ≥ 32 nm	*Summary of Issues*
Factory level and company wide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of high-aspect ratio technologies such as damascene challenges all metrology methods. Key requirements are dimensional control, void detection in copper lines, and pore size distribution and detection of killer pores in patterned low-κ dielectrics.	New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures in new low-κ dielectrics. Sidewall roughness impacts barrier integrity and the electrical properties of lines and vias.
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates. The same is true for measurement of barrier layers. Metal gate work function characteization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. There is a concern that measurements on test structures located in scribe lines do not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 32 nm	
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks.
Statistical limits of sub-32 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for ***beyond CMOS.***	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

** SPC—statistical process control parameters are needed to replace inspection, reduce process variation, control defects, and reduce waste.*

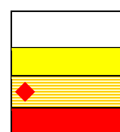
Table 117a Metrology Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*	
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*	
Microscopy										
Inline, nondestructive microscopy process resolution (nm) for P/T=0.1	**0.29**	**0.25**	**0.22**	**0.2**	**0.18**	**0.16**	**0.14**	**0.13**	**0.12**	*MPU Gate*
Microscopy capable of measurement of patterned wafers having maximum aspect ratio/diameter (nm) (DRAM contacts) [A]	**15**	**16**	**16**	**17**	**17**	**>20**	**>20**	**>20**	**>20**	*D1/2*
	95	**85**	**76**	**67**	**60**	**50**	**40**	**35**	**30**	
Materials and Contamination Characterization										
Real particle detection limit (nm) [B]	**32**	**28**	**25**	**22**	**20**	**18**	**16**	**14**	**13**	*MPU*
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	**27**	**23**	**22**	**19**	**17**	**15**	**13**	**12**	**11**	*D1/2*
Specification limit of total surface contamination for critical GOI surface materials (atoms/cm^2) [C]	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	*MPU Gate*
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	*MPU Gate*

Table 117b Metrology Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*Driver*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*	
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*	
Microscopy								
Inline, nondestructive microscopy process resolution (nm) for P/T=0.1	**0.1**	**0.09**	**0.08**	**0.07**	**0.06**	**0.06**	**0.05**	*MPU Gate*
Microscopy capable of measurement of patterned wafers having maximum aspect ratio/diameter (nm) (DRAM contacts) [A]	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**	**>20**	*D1/2*
	28	**25**	**23**	**20**	**18**	**16**	**14**	
Materials and Contamination Characterization								
Real particle detection limit (nm) [B]	**11**	**10**	**9**	**8**	**7**	**6**	**6**	*MPU*
Minimum particle size for compositional analysis (dense lines on patterned wafers) (nm)	**9**	**8**	**7**	**6**	**6**	**5**	**5**	*D1/2*
Specification limit of total surface contamination for critical GOI surface materials (atoms/cm^2) [C]	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	**5.00E+09**	*MPU Gate*
Surface detection limits for individual elements for critical GOI elements (atoms/cm^2) with signal-to-noise ratio of 3:1 for each element	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	**5.00E+08**	*MPU Gate*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 117a and b:
[A] Metal and via aspect ratios are additive for dual-Damascene process flow.
[B] This value depends on surface microroughness and layer composition.
[C] The requirements for metal contamination have been changed based on less stringent requirements found in Front End Processes chapter Surface Preparation Technology Requirements table, Note F.

Table 118a Lithography Wafer Metrology Technology Requirements—Near-term Years UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	Flash ½ Pitch (nm) (Un-contacted Poly)	*76*	*64*	*57*	*51*	*45*	*40*	*36*	*32*	*28*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
WAS	Printed gate CD control (nm) Uniformity (variance) is 12% of CD Allowed lithography variance = 3/4 total variance of physical gate length *	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.4
	Wafer dense line CD control (nm) * Uniformity is 13.5% of CD Allowed lithography variance = 3/4 total variance	8.8	7.4	6.6	5.9	5.3	4.7	4.2	3.7	3.3
	Wafer minimum contact hole (nm, post etch) from lithography tables	85	72	64	57	51	45	40	36	32
	Wafer contact CD control (nm)* Uniformity is 15% of CD = minimum contact hole size Allowed lithography variance = 2/3 total variance	10.4	8.8	7.8	7	6.2	5.5	4.9	4.4	3.9
WAS	Line width roughness (nm, 3 σ) < 8% of CD ***	2.6	2.2	2	1.8	1.6	1.4	1.3	1.1	1
IS	**Etched Gate Line Width Roughness (nm, 3 σ) < 8% of CD** ***	2.6	2.2	2	1.8	1.6	1.4	1.3	1.1	1
WAS	Wafer CD metrology tool precision (nm) * 3σ at P/T = 0.2 for isolated printed and physical lines [A]	0.67	0.58	0.52	0.46	0.42	0.37	0.33	0.29	0.27
IS	Wafer CD metrology tool precision (nm) * 3σ at P/T = 0.2 for isolated printed and physical lines [A]	0.67	0.58	0.52	0.46	0.42	0.37	0.33	0.29	0.27
WAS	Wafer CD metrology tool precision (nm) * (P/T=.2 for dense lines**)	1.77	1.49	1.33	1.18	1.05	0.94	0.84	0.74	0.66
IS	Wafer CD metrology tool precision (nm) * (P/T = .2 for dense lines**)	1.77	1.49	1.33	1.18	1.05	0.94	0.84	0.74	0.66
WAS	Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)****	2.08	1.76	1.57	1.4	1.25	1.1	0.98	0.88	0.78
IS	Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)****	2.08	1.76	1.57	1.4	1.25	1.1	0.98	0.88	0.78
WAS	Wafer CD metrology tool precision (nm) * (P/T=.2) for LWR***	0.52	0.44	0.4	0.36	0.32	0.28	.25	0.22	0.2
IS	Wafer CD metrology tool precision (nm) * (P/T=.2) for LWR***	0.52	0.44	0.4	0.36	0.32	0.28	0.25	0.22	0.2
	Maximum CD measurement bias (%)	10	10	10	10	10	10	10	10	10
	Aspect Ratio Capability for Trench Structure CD Metrology	15:01	15:01	15:01	15:01	15:01	15:01	15:01	15:01	20:01
	Wafer overlay control (nm)	15	13	11	10	9	8	7.1	6.4	5.7
	Wafer overlay output metrology precision (nm, 3 σ)* P/T=.1	1.51	1.27	1.13	1.01	0.9	0.8	0.71	0.64	0.57

** All precision values are 3 Sigma in nm and include metrology tool-to-tool matching. Requirement is for precision value at top, middle, and bottom CD.*
*** Measurement tool performance needs to be independent of target shape, material, and density.*
**** The Lithography roadmap has changed from line edge roughness (LER) to line width roughness (LWR).*
LER—Local line-edge variation (3 sigma total, all frequency components included, both edges) evaluated along a distance that allows determination of spatial wavelength equal to two times the technology generation dimension. LWR is defined as LWR=sqrt(2)LER for uncorrelated line edge roughness.
***** Bottom CD for contacts presently requires measurement by FIB.*

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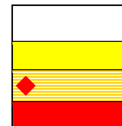

Table 118b Lithography Wafer Metrology Technology Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	Flash ½ Pitch (nm) (Un-contacted Poly)	*25*	*23*	*20*	*18*	*16*	*14*	*13*
	MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
WAS	Printed gate CD control (nm) Uniformity (variance) is 12% of CD Allowed lithography variance = 3/4 total variance of physical gate length *	1.1	1	0.9	0.8	0.7	0.6	0.6
IS	Printed gate CD control (nm) Uniformity (variance) is 12% of CD Allowed lithography variance = 3/4 total variance of physical gate length *	1.2	1	0.9	0.8	0.7	0.7	0.6
	Wafer dense line CD control (nm) * Uniformity is 13.5% of CD Allowed lithography variance = 3/4 total variance	3	2.6	2.3	2.1	1.9	1.7	1.5
	Wafer minimum contact hole (nm, post etch) from lithography tables	28	25	23	20	18	16	14
	Wafer contact CD control (nm)* Uniformity is 15% of CD = minimum contact hole size Allowed lithography variance = 2/3 total variance	3.4	3.1	2.8	2.4	2.2	2	1.7
WAS	Line width roughness (nm, 3 σ) < 8% of CD ***	.9	0.8	0.7	.6	0.6	.5	.5
IS	**Etched Gate Line Width Roughness (nm, 3 σ) < 8% of CD *** **	.9	0.8	0.7	.6	0.6	.5	.5
	Wafer CD metrology tool precision (nm) * 3σ at P/T = 0.2 for isolated printed and physical lines [A]	0.23	0.21	0.19	0.17	0.15	0.12	0.12
	Wafer CD metrology tool precision (nm) * (P/T = .2 for dense lines**)	0.59	0.53	0.47	0.42	0.37	0.33	0.3
	Wafer CD metrology tool precision (nm) * (P/T=.2 for contacts**)****	0.69	0.61	0.56	0.49	0.44	0.39	0.34
WAS	Wafer CD metrology tool precision (nm) * (P/T=.2) for LWR***	.18	0.16	0.14	.13	0.12	.1	.1
IS	Wafer CD metrology tool precision (nm) * (P/T=.2) for LWR***	0.18	0.16	0.14	0.13	0.12	0.1	0.1
	Maximum CD measurement bias (%)	10	10	10	10	10	10	10
	Aspect Ratio Capability for Trench Structure CD Metrology	20:01	20:01	20:01	20:01	20:01	20:01	20:01
	Wafer overlay control (nm)	5.1	4.5	4	3.6	3.2	2.8	2.5
	Wafer overlay output metrology precision (nm, 3 σ)* P/T=.1	0.51	0.45	0.4	0.36	0.32	0.28	0.25

** All precision values are 3 Sigma in nm and include metrology tool-to-tool matching. Requirement is for precision value at top, middle, and bottom CD.*
*** Measurement tool performance needs to be independent of target shape, material, and density.*
**** The Lithography roadmap has changed from line edge roughness (LER) to line width roughness (LWR).*
LER—Local line-edge variation (3 sigma total, all frequency components included, both edges) evaluated along a distance that allows determination of spatial wavelength equal to two times the technology generation dimension. LWR is defined as LWR=sqrt(2)LER for uncorrelated line edge roughness.
***** Bottom CD for contacts presently requires measurement by FIB.*

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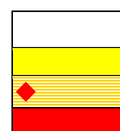


Table 119a Lithography Metrology (Mask) Technology Requirements: Optical—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU gate in resist (nm)	*54*	*48*	*42*	*38*	*34*	*30*	*27*	*24*	*21*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Flash ½ Pitch (nm) (Un-contacted Poly)	**76**	**64**	**57**	**51**	**45**	**40**	**36**	**32**	**28**
DRAM/Flash CD control (3sigma) (nm)	**8.8**	**7.4**	**6.6**	**5.9**	**5.3**	**4.7**	**4.2**	**3.7**	**3.3**
CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	**3.8**	**3.4**	**3.0**	**2.6**	**2.4**	**2.2**	**1.9**	**1.7**	**1.6**
Wafer overlay control (nm)	**15**	**13**	**11**	**10**	**9**	**8**	**7**	**6**	**6**
DRAM Contact after etch (nm)	**85**	**72**	**64**	**57**	**51**	**45**	**40**	**36**	**32**
Wafer contact CD control (nm)* Uniformity is 13.5% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	**10.0**	**8.4**	**7.5**	**6.6**	**5.9**	**5.3**	**4.7**	**4.2**	**3.7**
Mask nominal image size (nm) [B]	**214**	**191**	**170**	**151**	**135**	**120**	**107**	**95**	**85**
Mask minimum primary feature size [D]	**150**	**133**	**119**	**106**	**94**	**84**	**75**	**67**	**59**
Optical Section									
Minimum OPC size (opaque at 4×, nm) [D]	**90**	**80**	**70**	**64**	**56**				
Image placement (nm, multi-point) [F]	**9**	**8**	**7**	**6.1**	**5.4**	**4.8**	**4.3**	**3.8**	**3.4**
CD uniformity allocation to mask (assumption)	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
Mask error factor (MEF) from lithography tables isolated lines, binary	**1.4**	**1.4**	**1.6**	**1.8**	**2**	**2.2**	**2.2**	**2.2**	**2.2**
MEEF dense lines, binary or attenuated phase shift mask [G]	**2**	**2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
MEF contacts [G]	**3**	**3**	**3.5**	**4**	**4**	**4**	**4**	**4**	**4**
CD Uniformity (3 Sigma at 4×, nm) Refer to Lithography Chapter Table for Optical Mask Requirements									
Mask CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	**3.8**	**3.3**	**2.6**	**2.0**	**1.7**	**1.4**	**1.2**	**1.1**	**1.0**
Mask CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	**7.1**	**6.0**	**4.8**	**4.3**	**3.8**	**3.4**	**3.0**	**2.7**	**2.4**
Mask contact CD control (nm)* Uniformity is 12% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	**4.7**	**4.0**	**3.0**	**2.4**	**2.1**	**1.9**	**1.7**	**1.5**	**1.3**
Mask image placement metrology (precision, P/T=0.1)	**0.9**	**0.8**	**0.7**	**0.6**	**0.5**	**0.5**	**0.4**	**0.4**	**0.3**
Mask CD precision (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H] (P/T=0.2 for isolated lines, binary**)	**0.8**	**0.7**	**0.5**	**0.4**	**0.3**	**0.3**	**0.2**	**0.2**	**0.2**
Mask CD precision (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	**1.4**	**1.2**	**0.96**	**0.86**	**0.77**	**0.68**	**0.61**	**0.54**	**0.48**
Mask contact CD precision(nm)* Uniformity is 12% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	**0.9**	**0.8**	**0.6**	**0.5**	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**
Specific Requirements									
Alternated PSM phase mean deviation	**2**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**
Phase metrology precision, P/T=0.2	**0.4**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**	**0.2**
Attenuated PSM phase mean deviation from 180° (± degree) [S]	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**	**3**
Phase uniformity metrology precision, P/T=0.2	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**	**0.6**

Table 119b Lithography Metrology (Mask) Technology Requirements: Optical—Long-term Years

Optical Masks not part of potential solutions beyond 22 nm, grey-colored cells indicate the transition

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU gate in resist (nm)	*19*	*17*	*15*	*13*	*12*	*11*	*9*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Flash ½ Pitch (nm) (Un-contacted Poly)	**25**	**23**	**20**	**18**	**16**	**14**	**13**
DRAM/Flash CD control (3sigma) (nm)	**3.0**	**2.6**	**2.3**	**2.1**	**1.9**	**1.7**	**1.5**
CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	**1.3**	**1.2**	**1.1**	**1.0**	**0.8**	**0.7**	**0.7**
Wafer overlay control (nm)	**5**	**5**	**4**	**4**	**3**	**3**	**3**
DRAM Contact after etch (nm)	**28**	**25**	**23**	**20**	**18**	**16**	**14**
Wafer contact CD control (nm)* Uniformity is 13.5% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	**3.3**	**3.0**	**2.6**	**2.3**	**2.1**	**1.9**	**1.7**
Mask nominal image size (nm) [B]	**76**	**67**	**60**	**54**	**48**	**42**	**38**
Mask minimum primary feature size [D]	**53**	**47**	**42**	**37**	**33**	**30**	**26**
Optical Section							
Minimum OPC size (opaque at 4×, nm) [D]							
Image placement (nm, multi-point) [F]	**3.0**	**2.7**	**2.4**	**2.1**	**1.9**	**1.7**	**1.5**
CD uniformity allocation to mask (assumption)	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
Mask error factor (MEF) from lithography tables isolated lines, binary	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
MEEF dense lines, binary or attenuated phase shift mask [G]	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
MEF contacts [G]	**4**	**4**	**4**	**4**	**4**	**4**	**4**
CD Uniformity (3 Sigma at 4×, nm) Refer to Lithography Chapter Table for Optical Mask Requirements							
Mask CD uniformity (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H]	**0.8**	**0.8**	**0.7**	**0.6**	**0.5**	**0.5**	**0.5**

Table 119b Lithography Metrology (Mask) Technology Requirements: Optical—Long-term Years (continued)

Optical Masks not part of potential solutions beyond 22 nm, grey-colored cells indicate the transition

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU gate in resist (nm)	*19*	*17*	*15*	*13*	*12*	*11*	*9*
Mask CD uniformity (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	2.1	1.9	1.7	1.5	1.4	1.2	1.1
Mask contact CD control (nm)* Uniformity is 12% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	1.2	1.1	0.9	0.8	0.7	0.7	0.6
Mask image placement metrology (precision, P/T=0.1)							
Mask CD precision (nm, 3 sigma) isolated lines (MPU gates), binary or attenuated phase shift mask [H] (P/T=0.2 for isolated lines, binary**)	0.2	0.2	0.1	0.1	0.1	0.1	0.1
Mask CD precision (nm, 3 sigma) dense lines (DRAM half pitch), binary or attenuated phase shift mask [J]	0.43	0.38	0.34	0.30	0.27	0.24	0.21
Mask contact CD precision(nm)* Uniformity is 12% of CD = minimum contact hole size Allowed lithography variance = 3/4 total variance	0.2	0.2	0.2	0.2	0.1	0.1	0.1
Specific Requirements							
Alternated PSM phase mean deviation							
Phase metrology precision, P/T=0.2							
Attenuated PSM phase mean deviation from 180° (± degree) [S]	3	3	3				
Phase uniformity metrology precision, P/T=0.2	0.6	0.6	0.6				

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

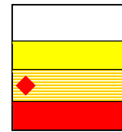


Table 119c Lithography Metrology (Mask) Technology Requirements: EUV—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Flash ½ Pitch (nm) (Un-contacted Poly)				**51**	**45**	**40**	**36**	**32**	**28**
Image placement error (nm, multipoint)				**6.1**	**5.4**	**4.8**	**4.3**	**3.8**	**3.4**
CD Uniformity (3 sigma at 4×, nm)									
Isolated lines (MPU gates) Uniformity is 10% of CD Mask error factor varies with year				**3.4**	**3.0**	**2.7**	**2.4**	**2.1**	**1.9**
Dense lines (DRAM half-pitch) Uniformity is 15% of CD Mask error factor varies with year				**8.2**	**7.3**	**6.5**	**5.8**	**5.2**	**4.6**
DRAM contact after Etch				**57**	**51**	**45**	**40**	**36**	**32**
Contact/Vias Uniformity is 10% of CD mask error factor varies with year				**7.6**	**6.8**	**4.8**	**4.3**	**3.8**	**3.4**
Mask CD metrology tool precision* (P/T=0.2 for isolated lines)**				**0.68**	**0.61**	**0.54**	**0.48**	**0.43**	**0.38**
Mask CD metrology tool precision* (P/T=0.2 for dense lines)**				**1.6**	**1.5**	**1.3**	**1.2**	**1.0**	**0.92**
Mask CD metrology tool precision* (P/T=0.2 for contact/vias)**				**1.5**	**1.4**	**1.0**	**0.86**	**0.76**	**0.68**
Specific Requirements									
Mean peak reflectivity				**65%**	**66%**	**66%**	**66%**	**67%**	**67%**
Peak reflectivity uniformity (3 sigma %)				**0.69%**	**0.58%**	**0.47%**	**0.42%**	**0.37%**	**0.33%**
Absorber sidewall angle tolerance (degrees)				**1**	**1**	**0.75**	**0.69**	**0.62**	**0.5**
Absorber LER (3 sigma, nm)				**3.2**	**2.8**	**2.5**	**2.2**	**2.0**	**1.8**
Mask substrate flatness (peak-to-valley, nm)				**75**	**60**	**50**	**41**	**36**	**32**
Metrology mean peak reflectivity precision (P/T=0.2, %)				**1.30%**	**1.30%**	**1.30%**	**1.30%**	**1.30%**	**1.30%**
Peak reflectivity uniformity metrology precision (3 sigma, P/T = 0.2)				**0.14%**	**0.12%**	**0.09%**	**0.08%**	**0.07%**	**0.07%**
Absorber sidewall angle metrology precision (degrees 3 sigma, P/T = 0.2)				**0.20**	**0.20**	**0.15**	**0.14**	**0.12**	**0.10**
Absorber LER metrology precision (3 sigma, P/T=0.2)				**0.64**	**0.57**	**0.50**	**0.45**	**0.40**	**0.36**
Mask substrate flatness metrology precision (nm 3 sigma, P/T=0.2)				**15**	**12**	**10**	**8.2**	**7.3**	**6.5**

Before 22 nm; grey-colored cells indicate the transition to EUV technology.

**All precision values are 3 sigma in nm and include metrology tool-to-tool matching.*
***Measurement tool performance needs to be independent of target shape, material, and density.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

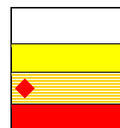


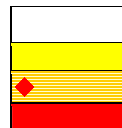
Table 119d Lithography Metrology (Mask) Technology Requirements: EUV—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Flash ½ Pitch (nm) (Un-contacted Poly)	**25**	**23**	**20**	**18**	**16**	**14**	**13**
Image placement error (nm, multipoint)	**3**	**2.7**	**2.4**	**2.1**	**1.9**	**1.7**	**1.5**
CD Uniformity (3 sigma at 4×, nm)							
Isolated lines (MPU gates) Uniformity is 10% of CD Mask error factor varies with year	**1.7**	**1.5**	**1.3**	**1.2**	**1.1**	**1.0**	**0.9**
Dense lines (DRAM half-pitch) Uniformity is 15% of CD Mask error factor varies with year	**4.1**	**3.7**	**3.3**	**2.9**	**2.6**	**2.3**	**2.1**
DRAM contact after Etch	**28**	**25**	**23**	**20**	**18**	**16**	**14**
Contact/Vias Uniformity is 10% of CD mask error factor varies with year	**3.0**	**2.7**	**1.8**	**1.6**	**1.4**	**1.3**	**1.1**
Mask CD metrology tool precision* (P/T=0.2 for isolated lines)**	**0.34**	**0.30**	**0.27**	**0.24**	**0.21**	**0.19**	**0.17**
Mask CD metrology tool precision* (P/T=0.2 for dense lines)**	**0.82**	**0.73**	**0.65**	**0.58**	**0.52**	**0.46**	**0.41**
Mask CD metrology tool precision* (P/T=0.2 for contact/vias)**	**0.61**	**0.54**	**0.36**	**0.32**	**0.29**	**0.26**	**0.23**
Specific Requirements							
Mean peak reflectivity	**67%**	**67%**	**67%**	**67%**	**67%**	**67%**	**67%**
Peak reflectivity uniformity (3 sigma %)	**0.29%**	**0.26%**	**0.23%**	**0.21%**	**0.19%**	**0.17%**	**0.15%**
Absorber sidewall angle tolerance (degrees)	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Absorber LER (3 sigma, nm)	**1.6**	**1.4**	**1.3**	**1.1**	**1.0**	**0.9**	**0.8**
Mask substrate flatness (peak-to-valley, nm)	**29**	**26**	**23**	**20**	**18**	**16**	**14**
Metrology mean peak reflectivity precision (P/T=0.2, %)	**1.30%**	**1.30%**	**1.30%**	**1.30%**	**1.30%**	**1.30%**	**1.30%**
Peak reflectivity uniformity metrology precision (3 sigma, P/T = 0.2)	**0.06%**	**0.05%**	**0.05%**	**0.04%**	**0.04%**	**0.03%**	**0.03%**
Absorber sidewall angle metrology precision (degrees 3 sigma, P/T = 0.2)	**0.10**	**0.10**	**0.10**	**0.10**	**0.10**	**0.10**	**0.10**
Absorber LER metrology precision (3 sigma, P/T=0.2)	**0.32**	**0.28**	**0.25**	**0.22**	**0.20**	**0.18**	**0.16**
Mask substrate flatness metrology precision (nm 3 sigma, P/T=0.2)	**5.8**	**5.1**	**4.6**	**4.1**	**3.6**	**3.2**	**2.9**

Grey cells indicate transition years of technologies.

**All precision values are 3 sigma in nm and include metrology tool-to-tool matching.*
***Measurement tool performance needs to be independent of target shape, material, and density.*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 119 a and b:
[A] The designation for CD measurement for isolated lines in the near term is a result of roadmap process range and the need for tool matching in the precision requirement makes this requirement very difficult to achieve. A work-around for isolated line CD measurement is to use a single tool and avoid tool matching. Long term, CD measurement for 25 nm linewidths requires a technology breakthrough because extension of known methods may not be possible.
[B] Mask Nominal Image Size—Equivalent to wafer minimum feature size in resist multiplied by the mask reduction ratio that equals 4×.
[C] Mask Minimum Primary Feature Size—Minimum printable feature after OPC application to be controlled on the mask for CD placement and defects.
[D] Mask OPC Feature size—Minimum width of the smallest non-printing features on the mask.

[E] The CD process range for isolated gate lithography is 4/5 of the total CD process range of 1/10 the CD at 3σ.
The CD process range is 4/5 of the 15% of CD for dense lines and 2/3 the 15% for contact/via. Process ranges are variances. It is important to note that the mask part of the lithography process range is allowed 40% of the total lithography process range. The mask error factor (MEF) reduces the CD process range, and its effect is calculated by dividing the process range by the MEF.
[F] The mask error factor for isolated lines on a binary mask changes from 1.4 to 1.6 at 65 nm.
[G] The mask error factor for alternating phase shift masks is 1.
[H] The mask error factor for dense lines is 2 from the 100nm to 70 nm . It is 2.5 at 65 nm, and is 3 for 57 and 50 nm.
[I] The mask error factor for contact and via lines is 3 from the 100nm to 70 nm. It is 3.5 at 65 nm, and is 4 for 57 and 50 nm.

Table 120a Front End Processes Metrology Technology Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
	Metrology for metal gate thickness and composition*									
	Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	$0.5x10^{10}$	$0.5x10^{10}$	$0.5x10^{10}$	$0.5x10^{10}$	$0.5x10^{10}$	$0.5x10^{10}$	$0.5x10^{10}$	$0.5x10^{10}$	$0.5x10^{10}$
	Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	$0.5x10^9$	$0.5x10^9$	$0.5x10^9$	$0.5x10^9$	$0.5x10^9$	$0.5x10^9$	$0.5x10^9$	$0.5x10^9$	$0.5x10^9$
Was	High-performance EOT (Extended planar bulk)	1.2	1.1	1.1	0.9	0.75	0.65	0.5	0.5	
IS	High-performance EOT (Extended planar bulk) for MPU/ASIC for 1.5E20 doped Poly-Si	1.2	1.1	1.1	1	0.9	~~0.65~~	~~0.5~~	~~0.5~~	
Was	High-performance EOT (FDSOI)				0.9	0.8	0.7	0.6	0.5	0.5
IS	High-performance EOT (FDSOI) MPU/ASIC for metal gate				0.9	0.8	0.7	0.6	0.5	0.5
Was	High-performance EOT (DG)							0.8	0.7	0.6
IS	High-performance EOT (multi-gate) MPU/ASIC for metal gate							0.8	0.7	0.6
Was	Low power EOT (bulk)	1.4	1.3	1.2	1.1	1	0.9	0.9	0.9	
IS	Low operating power EOT (bulk) for 1.5E20 doped poly-Si	1.4	1.3	1.2	1.1	1	0.6	0.6	0.6	
WAS	Low power EOT (DG)							0.9	0.9	0.8
IS	Low operating power EOT (multi gate and metal-gate)							0.9	0.9	0.8
WAS	Low power EOT (FD)							0.9	0.9	0.8
IS	Low operating power EOT (FD-SOI) (metal gate)							0.9	0.9	0.8
	$\pm 3\sigma$ dielectric process range (EOT) (nm)	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%
WAS	EOT measurement precision 3σ (nm) [B]	0.0048	0.0044	0.0044	0.0036	0.003	0.0026	0.002	0.002	0.002
IS	EOT measurement precision 3σ (nm) [B]	0.0048	0.0044	0.0044	0.004	0.0036	0.0024	0.0024	0.002	0.002
ADD	Gate Dielectric Elemental Composition including Nitrogen Concentration Metrology for Patterned Wafers Precision (at %)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
	DRAM stacked capacitor structure including electrodes	Cylinder/ Pedestal MIM	Cylinder/ Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM/ others	Pedestal MIM	Pedestal MIM/ others	Pedestal MIM/ others
	DRAM stacked capacitor electrodes (near term)	MIM	MIM	MIM	MIM	MIM	MIM	MIM	MIM	MIM
WAS	DRAM stacked capacitor dielectric material	ALO/TAO /others	ALO/TAO /others	ALO/TAO /others	ALO/TAO /others	ALO/TAO /others	ALO/TAO /others	new material	new material	new material
IS	DRAM stacked capacitor dielectric material	AlO/TaO	AlO, HfO, TaO TiO, ZrO	AlO, HfO, TaO TiO, ZrO	AlO, HfO, TaO TiO, ZrO	AlO, HfO, TaO TiO, ZrO	AlO, HfO, TaO TiO, ZrO	Ultra-High K New Materials	Ultra-High K New Materials	Ultra-High K New Materials
	DRAM stacked capacitor dielectric constant	40	50	50	50	50	50	50	60	60
	EOT (nm) for stacked capacitor	1.8	1.4	0.8	0.8	0.8	0.7	0.7	0.6	0.5
	DRAM stacked capacitor dielectric physical thickness (nm)	18	17.5	10	10	10	8.75	8.75	9	7.5
	$\pm 3\sigma$ process range	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%
	DRAM capacitor dielectric physical thickness measurement precision (nm 3s) [C]	0.0072	0.0056	0.0032	0.0032	0.0032	0.0028	0.0028	0.0024	0.002
	Uniform channel concentration (cm^{-3}), for V_t=0.4 [W]	1.5–2.5 E18	2.0–4.0 E18	2.5–5.0 E18	NA	NA	NA	NA	NA	NA
	Dopant atom	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B
WAS	Metrology for junction depth [based on drain extension] of (nm) Note change to different structure for 2008	17.6	15.4	13.8	8.8	8	7.2	12.8	11.2	10.4
IS	Metrology for junction depth [based on drain extension] of (nm) Note change to different structure for 2008	11	9	7.5	7.5	7	6.5	5.8	4.5	
WAS	Extension lateral abruptness (nm/decade) [M]	3.5	3.1	2.8	TBD	TBD	TBD	TBD	TBD	TBD

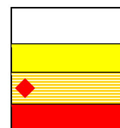
IS	*Extension lateral abruptness (nm/decade) [M]*	3.5	3.1	2.8	2.5	2.2	2	1.8	1.5	TBD
WAS	*Lateral/depth spatial resolution for 2D/3D dopant profile (nm)*	3.5	3.1	2.8	TBD	TBD	TBD	TBD	TBD	TBD
IS	*Lateral/depth spatial resolution for 2D/3D dopant profile (nm)*	3.5	3.1	2.8	2.5	2.2	2	1.8	1.5	TBD
	At-line dopant concentration precision (across concentration range) [D]	4%	4%	4%	4%	4%	2%	2%	2%	2%
WAS	*Metal gate work function for bulk MPU/ASIC |Ec,v – fm| (eV) [***]*		<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	
IS	*Metal gate work function for bulk MPU/ASIC |Ec,v – fm| (eV) [***]*		~~<0.2~~	~~<0.2~~	~~<0.2~~	~~<0.2~~	<0.2	<0.2	<0.2	
WAS	*Metal gate work function for FDSOI MPU/ASIC | fm – Ei| (eV)| NMOS/PMOS [***]*				± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1
IS	*Metal gate work function for FDSOI MPU/ASIC |ϕm – Ei| (eV)| NMOS/PMOS [***]*				~~± 0.1~~	~~± 0.1~~	± 0.15	± 0.15	± 0.15	± 0.15
	Metal gate work function for multi-gate MPU/ASIC [***]							midgap	midgap	midgap
WAS	*Metal gate work function for bulk low operating power |Ec,v – fm| (eV) [***]*		<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
IS	*Metal gate work function for bulk low operating power |Ec,v – fm| (eV) [***]*		~~<0.2~~	~~<0.2~~	~~<0.2~~	~~<0.2~~	<0.2	<0.2	<0.2	~~<0.2~~
DELETED	~~*Metal gate workfunction for FDSOI LOP [***]*~~	-	-		-	-	-	~~midgap~~	~~midgap~~	~~midgap~~
DELETED	~~*Metal gate work function for multi-gate LOP [***]*~~	-	-		-	-	-	~~midgap~~	~~midgap~~	~~midgap~~
ADD	***Metal gate workfunction for FDSOI and multi-gateLOP [***]***							midgap	midgap	midgap
WAS	*Metal gate work function for bulk LSTP |Ec,v – fm| (eV) [***]*				<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
IS	*Metal gate work function for bulk LSTP |Ec,v – ϕm| (eV) [***]*				<0.2	<0.2	<0.2	<0.2	<0.2	<0.2
WAS	*Metal gate work function for FDSOI and multi-gate LSTP | fm - Ei| (eV)| NMOS/PMOS [***]*									
IS	*Metal gate work function for FDSOI and multi-gate LSTP | ϕm - Ei| (eV)| NMOS/PMOS [***]*								+ / -0.1	+ / -0.1
	*Metrology for metal gate thickness and composition**									
ADD	***Elemental Composition Metrology for Metal Gate on Test Wafers Precision (at %)***	-	-	-	0.1	0.1	0.1	0.1	0.1	0.1
ADD	***Elemental Composition Metrology for Metal Gate on Patterned Wafers Precision (at %)***	-	-	-	0.1	0.1	0.1	0.1	0.1	0.1
	Starting silicon layer thickness (SOI) (fully depleted) (tolerance ± 5%, 3s) (nm) [M]	20–36	19–34	18–33	17–31	16–30	15–19	15–18	14–17	14–17
	SOI Si thickness precision (3s in nm)	0.1	0.095	0.09	0.085	0.08	0.075	0.075	0.07	0.07

Table 120b Front End Processes Metrology Technology Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	*Metrology for metal gate thickness and composition**							
	Bulk control limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}	0.5x10^{10}
	Bulk detection limits for trace metals for bulk silicon and SOI top silicon layer. (Fe concentration in atoms/cm^3)	0.5x10^9	0.5x10^9	0.5x10^9	0.5x10^9	0.5x10^9	0.5x10^9	0.5x10^9
	High-pPerformance EOT (Extended planar bulk)							
WAS	*High-performance EOT (FDSOI)*	0.5	0.5					
IS	*High-performance EOT (FDSOI) MPU/ASIC for Metal Gate*	0.5	0.5					
WAS	*High-performance EOT (DG)*	0.6	0.6	0.5	0.5	0.5	0.5	0.5
IS	*High-performance EOT (multi-gate) MPU/ASIC for metal Gate*	0.6	0.6	0.5	0.5	0.5	0.5	0.5
	Low power EOT (bulk)							
WAS	*Low power EOT (DG)*	0.8	0.8	0.7	0.7	0.7	0.7	0.7
IS	*Low operating power EOT (multi Gate and metal-Gate)*	0.8	0.8	0.7	0.7	0.7	0.7	0.7
WAS	*Low power EOT (FD)*	0.8	0.8	0.7	0.8			
IS	*Low operating power EOT (FD-SOI) (metal Gate)*	0.8	0.8	0.7	0.8			
	± 3σ dielectric process range (EOT) (nm)	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%	± 4%
	EOT measurement precision 3σ (nm) [B]	0.002	0.002	0.002	0.002	0.002	0.002	0.002
	DRAM stacked capacitor structure including electrodes	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM	Pedestal MIM
	DRAM stacked capacitor electrodes (near term)							
	DRAM stacked capacitor dielectric material	new material	new material					
	DRAM stacked capacitor dielectric constant	70	80	80	90	100		
	EOT (nm) for stacked capacitor	0.5	0.4	0.4	0.3	0.25		
	DRAM stacked capacitor dielectric physical thickness (nm)	8.75	8	8	6.75	6.25	0	0
	± 3 σ process range	± 4%	± 4%	± 4%	± 4%	± 4%		
	DRAM capacitor dielectric physical thickness measurement precision (nm 3s) [C]	0.002	0.0016	0.0016	0.0012	0.001	0	0
	Uniform channel concentration (cm^{-3}), for V_t=0.4 [W]	NA	NA	NA	NA	NA		
	Dopant atom	P, As, B	P, As, B	P, As, B	P, As, B	P, As, B		
WAS	*Metrology for junction depth [based on drain extension] of (nm) Note change to different structure for 2008*	8.8	8	7.2	6.4	5.6		
IS	*Metrology for junction depth [based on drain extension] of (nm) Note change to different structure for 2008*	~~8.8~~	~~8~~	~~7.2~~	~~6.4~~	~~5.6~~		
	Extension lateral abruptness (nm/decade) [M]	TBD	TBD	TBD	TBD	TBD		
	Lateral/depth spatial resolution for 2D/3D dopant profile (nm)	TBD	TBD	TBD	TBD	TBD		
	At-line dopant concentration precision (across concentration range) [D]	2%	2%	2%	2%	2%		
WAS	*Metal gate work function for bulk MPU/ASIC |Ec,v – fm| (eV) [***]*							
IS	*Metal gate work function for bulk MPU/ASIC |Ec,v – fm| (eV) [***]*							
WAS	*Metal gate work function for FDSOI MPU/ASIC | fm – Ei| (eV)| NMOS/PMOS [***]*	± 0.1	± 0.1					
IS	*Metal gate work function for FDSOI MPU/ASIC | fm – Ei| (eV)| NMOS/PMOS [***]*	± 0.15	± 0.15					
WAS	*Metal gate work function for multi-gate MPU/ASIC [***]*	midgap	midgap	midgap	midgap	midgap	midgap	midgap

IS	*Metal gate work function for multi-gate MPU/ASIC [***]*	midgap	midgap	midgap	midgap	midgap	midgap	midgap
WAS	*Metal gate work function for bulk low operating power |Ec,v – fm| (eV) [***]*							
IS	*Metal gate work function for bulk low operating power |Ec,v – fm| (eV) [***]*							
DELETED	~~*Metal gate work function for FDSOI LOP [***]*~~	~~midgap~~	~~midgap~~	~~midgap~~	~~midgap~~	~~midgap~~	~~midgap~~	~~midgap~~
DELETED	~~*Metal gate work function for multi-gate LOP [***]*~~	~~midgap~~	~~midgap~~	~~midgap~~	~~midgap~~	~~midgap~~	~~midgap~~	~~midgap~~
ADD	*Metal gate work function for FDSOI and multi-gate LOP [***]*	midgap	midgap	midgap	midgap	midgap	midgap	midgap
WAS	*Metal gate work function for bulk LSTP |Ec,v - fm| (eV) [***]*							
IS	*Metal gate work function for bulk LSTP |Ec,v - fm| (eV) [***]*							
WAS	*Metal gate work function for FDSOI and multi-gate LSTP | fm - Ei| (eV)| NMOS/PMOS [***]*	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1
IS	*Metal gate work function for FDSOI and multi-gate LSTP | fm - Ei| (eV)| NMOS/PMOS [***]*	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1	± 0.1
	Starting silicon layer thickness (SOI) (fully depleted) (tolerance ± 5%, 3s) (nm) [M]	13–16	13–15	13–15	12–14	12–14		
	SOI Si thickness precision (3s in nm)	0.065	0.065	0.065	0.06	0.06	0.1	0.1

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Table 120a and b:

[A] The use of SOI wafers requires metrology development.

[B] Precision calculated from P/T=0.1=6× precision/process range. The measurement requirements specify the equivalent thickness for a silicon dioxide dielectric film. It is expected that oxynitirides and stacked nitride/silicon dioxide layers will replace silicon dioxide for the 130 and 100 nm logic generations and that high dielectric constant materials such as Ta_2O_5 will be used at and after the 70 nm logic half pitch and possibly at 100 nm. The physical thickness of the high dielectric constant layer can be calculated by multiplying the ratio of the dielectric constants ($\varepsilon_{high-\kappa}/\varepsilon_{ox}$) by the effective oxide thickness. For example, a 6.4 nm thick Ta_2O_5 (κ= ~25) layer has a 1 nm equivalent oxide (κ =3.9) thickness. The listed precision is based on equivalent oxide thickness and must be multiplied by the ratio of the dielectric constant to obtain precision for the dielectric of interest. The total capacitance of the dielectric stack also includes that of the dielectric layer plus the interfacial layer, quantum state effects at the channel interface, and that associated with depletion of charge in the poly silicon gate electrode. Thus, the challenge to gate dielectric thickness measurement includes metrology for the interfacial layer.

[C] In the case of MIS structure, physical thickness, $t_{(diel)}$, is calculated using the equation of $t_{(diel)}=(t_{eq.ox}\text{-}1\ nm)_{diel}\ \varepsilon_{high-\kappa} / 3.9$ in which oxide film formed at the interface of poly-silicon and dielectric material in annealing is taken into account. In the case of MIM structure, t_{diel} is calculated using the equation of $t_{diel}= t_{eq.ox}\ \varepsilon_{high-\kappa} / 3.9$. Here teq.ox is equivalent oxide thickness, and t_{diel} is dielectric constant of the dielectric material.

[D] High- precision measurements with low systematic error are required.

Table 121a Interconnect Metrology Technology Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Metrology for maintaining planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm) [A]	500	500	500	500	500	500	500	500	500
Measurement of deposited barrier layer at thickness (nm)	7.3	6	5.2	4.3	3.7	3.3	2.9	2.6	2.4
Process range (± 3σ)	10%	10%	10%	10%	10%	10%	10%	10%	10%
Precision σs (nm) for P/T=0.1 [B]	0.073	0.06	0.052	0.043	0.037	0.033	0.029	0.026	0.024
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	24	21	19	17	15	14	13	13	10
Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1% or more of total metal level conductor volume of copper lines and vias.	8	7	6.5	5.7	5	4.5	4	3.5	3.2
Detection of killer pore in ILD at (nm) size	8	7	6.5	5.7	5	4.5	4	3.5	3.2
Measure interlevel metal insulator bulk/effective dielectric constant (κ) and anisotropy on patterned structures [C]	≤ 2.7	≤ 2.7	≤ 2.4	≤ 2.4	≤ 2.2	≤ 2.2	≤ 2.2	≤ 2.0	≤ 2.0
	3.1–3.4	3.1–3.4	2.7–3.0	2.7–3.0	2.5–2.8	2.5–2.8	2.5–2.8	2.3–2.6	2.3–2.6

Table 121b Interconnect Metrology Technology Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Metrology for maintaining planarity requirements: lithography field (mm × mm) for minimum interconnect CD (nm) [A]	500	500	500	500	500	500	500
Measurement of deposited barrier layer at thickness (nm)	2.1	1.9	1.7	1.5	1.3	1.2	1.1
Process range (± 3σ)	10%	10%	10%	10%	10%	10%	10%
Precision σs (nm) for P/T=0.1 [B]	0.021	0.019	0.017	0.015	0.013	0.012	0.011
Metrology capability to measure Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% areal density, 500 µm square array	10	9	8	7	7	6	6
Detection of post deposition and anneal process voids at or exceeding listed size (nm) when these voids constitute 1% or more of total metal level conductor volume of copper lines and vias.	2.8	2.5	2.2	2	1.8	1.6	1.4
Detection of killer pore in ILD at (nm) size	2.8	2.5	2.2	2	1.8	1.6	1.4
Measure interlevel metal insulator bulk/effective dielectric constant (κ) and anisotropy on patterned structures [C]	≤ 2.0	≤ 1.8	≤ 1.8	≤ 1.8	≤ 1.6	≤ 1.6	≤ 1.6
	2.3–2.6	2.1–2.4	2.1–2.4	2.1–2.4	1.9–2.2	1.9–2.2	1.9–2.2

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known