3-Bits/Cell NAND Flash

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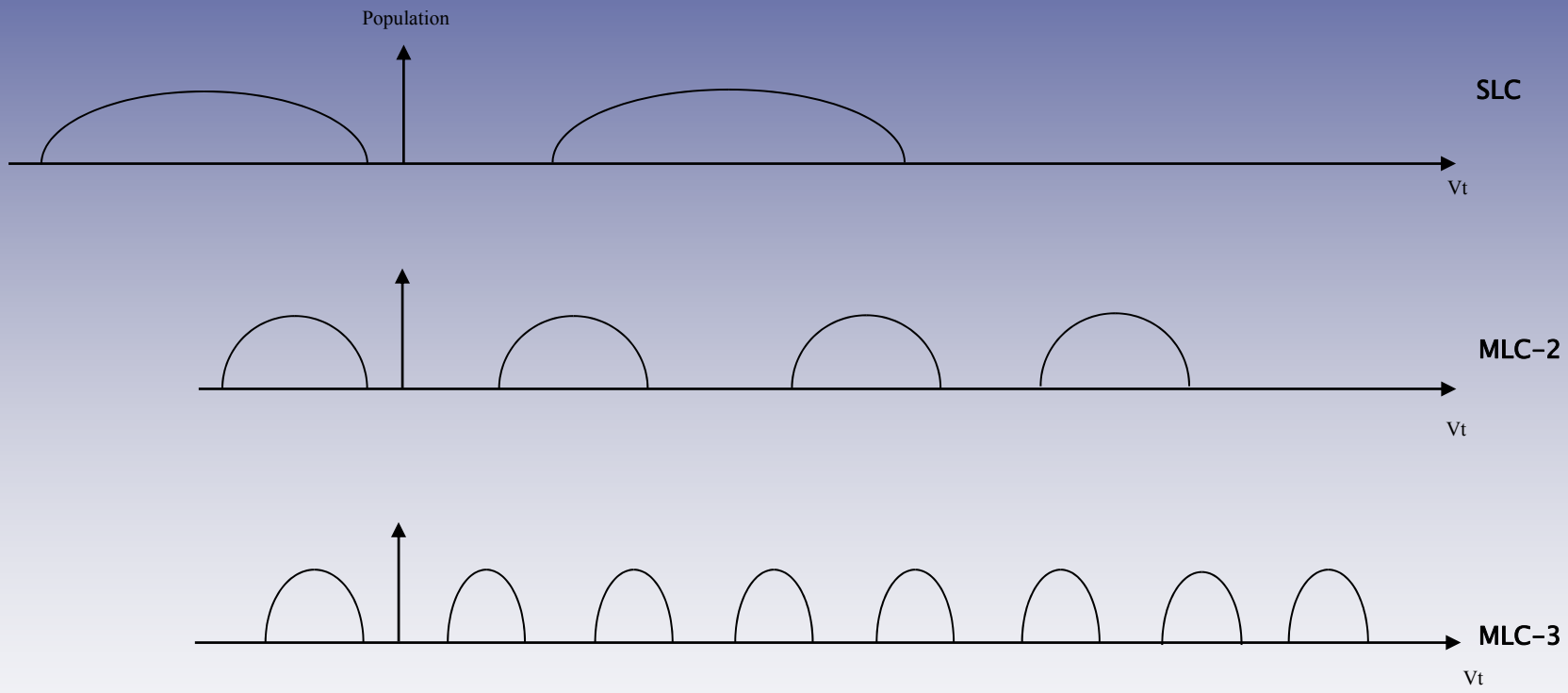
Agenda

- 3-bits/cell NAND Flash cost advantages
- Architecture
- Performance and endurance
- System requirements
- Applications suited to 3 BPC
- Summary

NAND Flash Cell Vt Distributions



Are There Cost Advantages to 3-Bits/Cell?

- With same process technology, 3-bits/cell technology provides more bits per wafer and lower cost per bit
- Delayed enablement of 3-bits/cell technology on leading edge process technology has allowed 2-bits/cell technology to stay ahead on costs
- Cost challenges exist when testing 3-bits/cell technology

Are There Cost Advantages to 3-Bits/Cell Technology?

- Traditionally, in the memory industry, costs have been reduced by enabling smaller process geometries
  - Still the case for NAND
  - We believe Micron's 34nm, 2-bits/cell technology device is leading the industry in overall cost per bit
  - Micron continues to see a viable shrink path in NAND for next several years

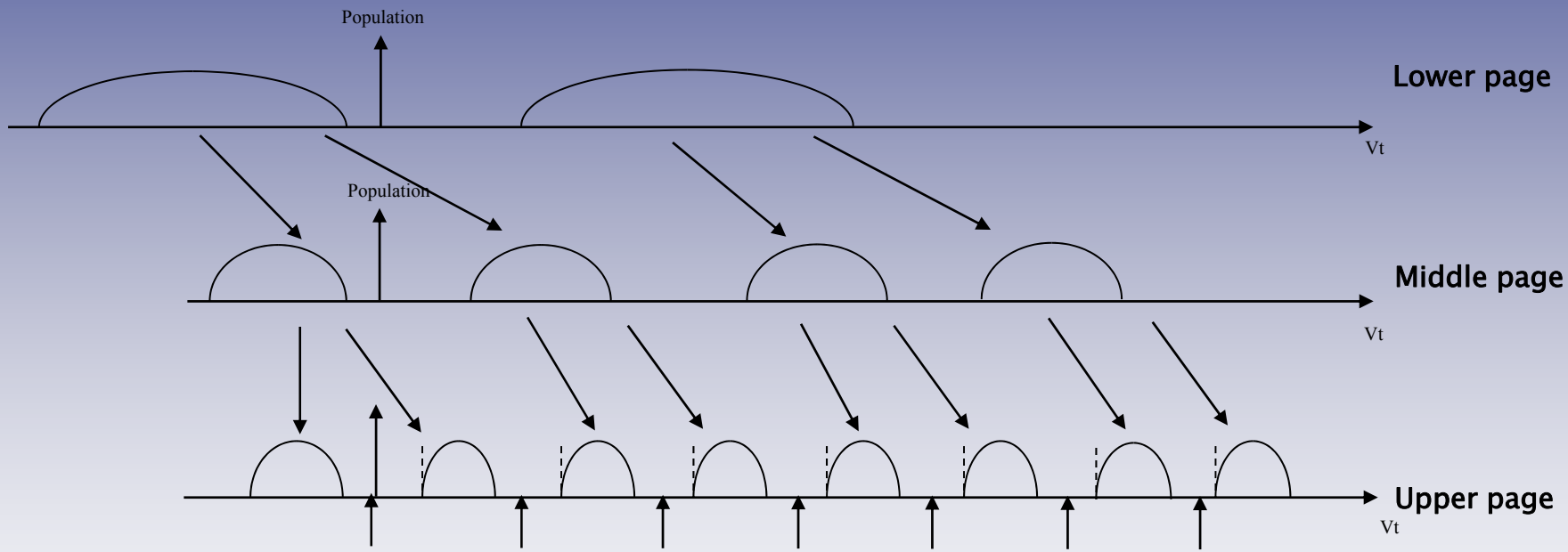
Why 3-Bits/Cell Technology?

- Micron is working on more 3-bits/cell technologies
- Will deploy based on whether they enable a cheaper cost per bit over the shrink path
- And provided the 3-bits/cell technology can meet the performance needs of the application

3-Bits/Cell Technology Architecture

- Like 2-bits/cell technology architecture, the pages in each block are shared within a cell
  - Lower page – Programs cells with first bit of information
  - Middle page – Programs cells with second bit of information
  - Upper page – Programs cells with third bit of information
- Results in 1.5X number of pages of 2-bits/cell technology architectures

Programming 3-Bits/Cell Technology



Why do Performance and Endurance Degrade with 3-Bits/Cell Technology?

- Due to high electrical fields and use of tunneling for program and erase, NAND cells intrinsically wear out
- Wear out of NAND cells results in significant variation in program and erase characteristics
- In addition to wear-out effects, intrinsic cell variation results in a wide range of program and erase characteristics across an array

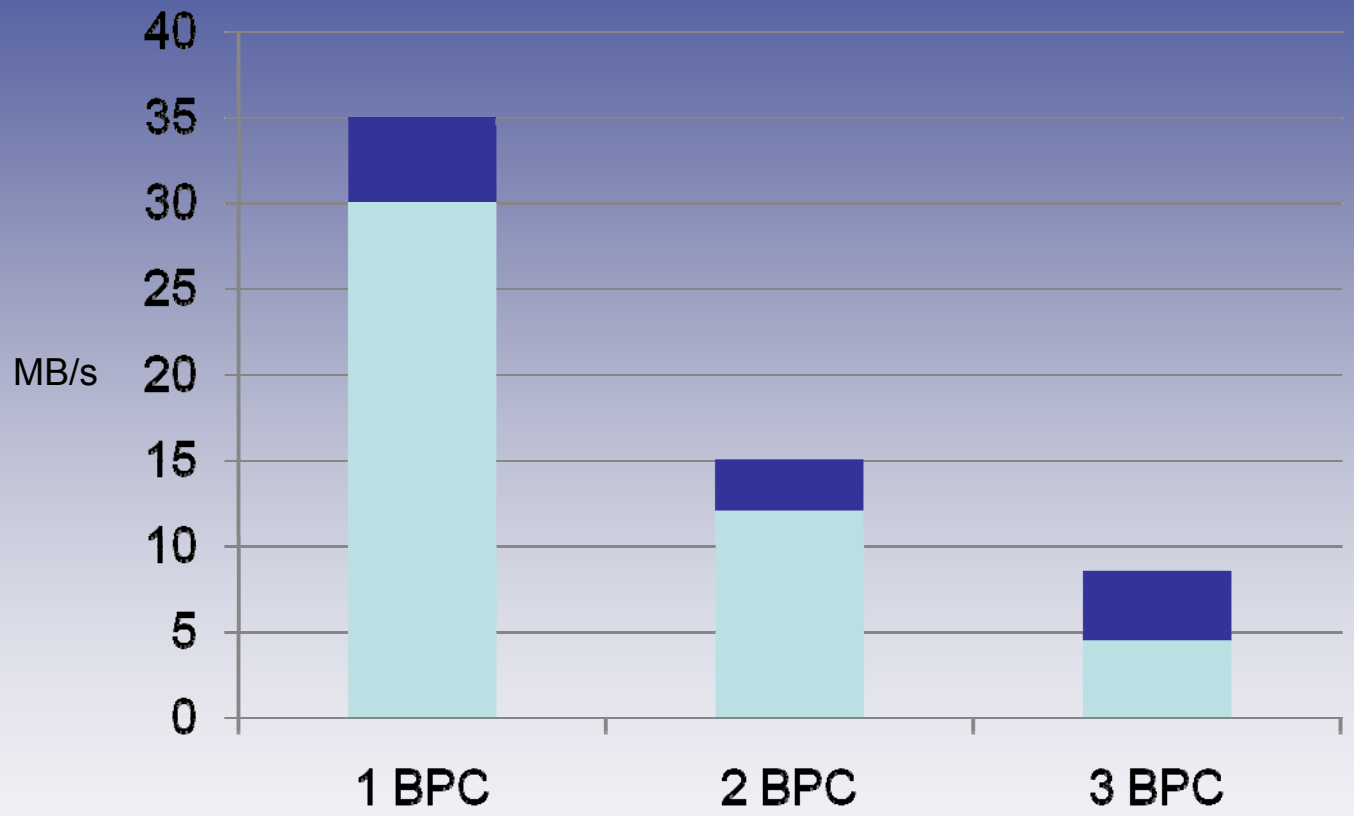
Why do Performance and Endurance Degrade with 3-Bits/Cell Technology?

- To manage sources of intrinsic cell variation, NAND designs implement iterative program and erase algorithms
- Due to finer placement Vt distributions required for 3-bits/cell technology, shorter and more iterations are needed
- This results in larger program and erase times

3-Bits/Cell Technology Performance

- Due to larger program window and decreased read window budget, program and read times will increase
- $^{t}PROG$
- ^{t}R
- Erase time
- Power consumption

Write Performance Ranges



Assumes multi-plane page programming, asynchronous data entry (^{t}WC = 20 NS)

3-Bits/Cell Technology Endurance

- Endurance of 3-bits/cell technology is greatly reduced due to:
  - Wear out of the NAND cells
  - Trapping of electrons
  - Finer placement of Vt cell distributions
- 3-bits/cell technology material endurance will be lower compared with 5K to 10K P/E cycles for 2-bits/cell technology

System Requirements for 3-Bits/Cell Technology

- Increased ECC
  - Increased codeword size: 512B -> 1KB -> 2KB
  - BCH or other advanced ECC algorithms
- Data scrambler
  - Due to array sensitivity to systematic data patterns, a data scrambler may be needed on the controller
- Embedded controller
  - May be needed and will become more critical as ECC requirements increase with 3-bits/cell technology and beyond

Applications Suited to 3-Bits/Cell Technology

- USB – good match
- PMP – good match if controller supports ECC requirement for 3-bits/cell technology
- SD – due to large block copy time with increased number of pages per block, requires more advanced firmware for improving performance and avoiding timeouts
- SSD – certain applications may work where performance is acceptable

Summary

- 3-bits/cell technology only has cost advantage over 2-bits/cell technology if the 3-bits/cell technology can be enabled before 2-bits/cell technology process shrinks
- Cost versus the endurance and performance of 3-bits/cell technology needs to considered
- 3-bits/cell technology performance and endurance limit the applications where it can be used