INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2006 UPDATE

MODELING AND SIMULATION

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MODELING AND SIMULATION

SUMMARY

Similar to the other chapters of the ITRS, in the Modeling and Simulation chapter only the tables have been revised in the 2006 Update. Important other developments like the further increasing interdependencies with the other chapters of the ITRS, e.g., concerning Design for Manufacturing, have been discussed but can and will only be presented in the next full version of the ITRS in 2007. This is intended to further promote the usefulness of Modeling and Simulation to improve the physical understanding in semiconductor technology and to reduce development times and costs.

Concerning the Modeling and Simulation challenges, only some details of the six short-term and the four long-term challenges for Modeling and Simulation were changed: Concerning the short-term challenges, lithography simulation was extended by the inclusion of multiple exposure/patterning, which has during the last months got high and urgent interest to enable the printing of smaller feature sizes. Electromagnetic field effects have been explicitly mentioned because their accurate treatment is getting indispensable for sufficiently accurate simulation. Ultimate nanoscale CMOS simulation capability was extended by the explicit inclusion of novel memory devices, such as magnetic RAM (MRAM) and programmable RAM (PRAM). Furthermore, reliability modeling for ultimate CMOS has been highlighted. Thermal-mechanical-electrical modeling for interconnections and packaging was extended to include 3D integration. Concerning the long-term challenges, nanoscale modeling was extended to explicitly include non-charge state devices, which are in detail discussed in the Emerging Research Devices (ERD) section of the ITRS. Optoelectronics modeling was extended to include optical couplers.

Whereas the fields of requirements have not changed, several details, including some timelines, were modified or added in view of the changes in industrial needs and state-of-the-art. Among the most significant changes is the more detailed requirement on the lithography options, referring especially to the several upcoming generations of immersion lithography. The newly required multiple exposure option especially affects resist modeling. For device modeling, updates refer especially to (quasi-)ballistic transport and quantum effects.

As with the long-term challenges, also for the long-term requirements interactions with the ERD and Emerging Research Materials (ERM) part of the ITRS increasingly get important. In the 2006 update this has been documented among others by the inclusion of ERD devices in the long-term requirements for Numerical Device Simulation.

Concerning the Modeling and Simulations requirements tables, an important change has been the separation between the absolute accuracy of a model or simulator (after calibration to a certain technology, e.g., one company's 90 nm technology), and the accuracy of the sensitivity with respect to technological input parameters. For example, if the critical dimension (CD) of a gate is changed due to a change in exposure dose, that CD change should be predicted by simulation with an error of less than 10%.

DIFFICULT CHALLENGES

Table 122 Modeling and Simulation Difficult Challenges UPDATED

Difficult Challenges ≥ 32 nm	*Summary of Issues*
High-frequency device and circuit modeling for 5–100 GHz applications	Efficient extraction and simulation of full-chip interconnect delay and power consumption Accurate and yet efficient 3D interconnect models, especially for transmission lines and S-parameters Extension of physical device models to III/V materials High-frequency circuit models including non-quasi-static effects, substrate noise, 1/f noise and parasitic coupling Parameter extraction assisted by numerical electrical simulation instead of RF measurement Scalable active and passive component models for compact circuit simulation Co-design between interconnects and packaging
Front-end process modeling for nanometer structures	Diffusion/activation/damage/stress models and parameters including SPER and low thermal budget processes in Si-based substrate, that is, Si, SiGe:C, Ge, SOI, epilayers, and ultra-thin body devices Modeling of epitaxially grown layers: Shape, morphology, stress Characterization tools/methodologies for ultra shallow geometries/junctions and low dopant level Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces Front-end processing impact on reliability
Integrated modeling of equipment, materials, feature scale processes and influences on devices	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms, and simplified but physical models for complex chemistry and plasma reaction Linked equipment/feature scale models (including high-κ metal gate integration, damage prediction) CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects) MOCVD, PECVD, ALD, electroplating and electroless deposition modeling Multi-generation equipment/wafer models

Table 122 Modeling and Simulation Difficult Challenges UPDATED (continued)

IS	Lithography simulation including NGL	Optical simulation of resolution enhancement techniques including mask optimization (OPC, PSM) Predictive resist models (e.g., mesoscale models) including line-edge roughness, etch resistance, adhesion, and mechanical stability Methods to easily calibrate resist model kinetic and transport parameters Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects Experimental verification and simulation of ultra-high NA vector models, including polarization effects from the mask and the imaging system Models and experimental verification of non-optical immersion lithography effects (e.g., topography and change of refractive index distribution) Simulation of multiple exposure/patterning Multi-generation lithography system models Simulation of defect influences/defect printing Modeling lifetime effects of equipment and masks
IS	Ultimate nanoscale device simulation capability	Methods, models and algorithms that contribute to prediction of CMOS limits General, accurate and computationally efficient quantum based simulators Models and analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS Models and analysis to investigate new memory devices like MRAM, PRAM, etc Gate stack models for ultra-thin dielectrics Models for device impact of statistical fluctuations in structures and dopant distribution Material models for stress engineering. Reliability modeling for ultimate CMOS Physical models for stress induced device performance
IS	Thermal-mechanical-electrical modeling for interconnections and packaging	Model thermal-mechanical, thermodynamic and electronic properties of low κ, high κ, and conductors for efficient in-chip package layout and power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension Model reliability of packages and interconnects incl. 3D integration (e.g., stress voiding, electromigration, piezoelectric effects; textures, fracture, adhesion) Models for electron transport in ultra fine patterned conductors.

Table 122 Modeling and Simulation Difficult Challenges UPDATED (continued)

	Difficult Challenges < 32 nm	*Summary of Issues*
	Modeling of chemical, thermomechanical, and electrical properties of new materials	Computational materials science tools to describe materials properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: Gate stacks, predictive modeling of dielectric constant, bulk polarization charge, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, reliability, breakdown, and leakage currents including band structure, tunneling from process/materials and structure conditions. Models for air gap and novel integrations in 3D interconnects including data for ultrathin material properties. Linkage with first principle computation and reduced model (classical MD or thermodynamic computation). Accumulation of databases for semi-empirical computation. Models for new ULK materials that are also able to predict process impact on their inherent properties.
	Prediction of dispersion of circuit parameters	Computer-efficient inclusion of influences of statistics (including correlations) before process freeze, quantum/ballistic transport, etc., into compact modeling Efficient extraction of circuit-level variations from process and device simulation
IS	Nano-scale modeling	Process modeling tools for the development of novel nanostructure devices (nanowires, carbon nanotubes (including doping), quantum dots, molecular electronics) Device modeling tools for analysis of nanoscale device operation (quantum transport, resonant tunneling, spintronics, contact effects - non charge-state devices)
IS	Optoelectronics modeling	Materials and process models for optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, optical interconnect models, semiconductor laser modeling. Physical design tools for integrated electrical/optical systems

TECHNOLOGY REQUIREMENTS

Table 123a Modeling and Simulation Technology Requirements: Capabilities—Near-term Years UPDATED

**For 2005/2006, interim solutions are known but research is still needed towards mature commercial solutions.*

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
	Lithography									
WAS	Exposure	**Simulation of immersion lithography including physical mask parameters, mask birefringence and mask polarization effects**		**Simulation of EUV, EPL, ML2, imprint lithography options, models bridging OPC and predictive feature scale simulation**					**NGL models and modeling of materials and components (immersion, EUV, EPL, ML2 lithographic processes, imprint)**	
IS	Exposure	**Simulation of immersion lithography including physical mask parameters, mask birefringence and mask polarization effects [1]**		**Simulation of immersion lithography for high NA liquids (NA about 1.5) [2]**		**Simulation of EUV, ~~EPL~~, very high NA (about 1.7), ML2, imprint lithography options, models bridging OPC and predictive feature scale simulation [3]**			**NGL models and modeling of materials and components (immersion, EUV, EPL, ML2 lithographic processes, imprint)**	
WAS	Resist models	**Detailed chemically amplified resist and EUV resist models including LER and immersion (liquid-solid interface), and methods to easily calibrate parameters; coupling with etch models**				**Finite polymer-size effects**		**Meso-scale resist models with finite molecule effects**		**Non-conventional photoresist models and coupling with etch models**
IS	Resist models	**Detailed chemically amplified resist and EUV resist models including LER and immersion (liquid-solid interface), and methods to easily calibrate parameters; coupling with etch models**			**Multiple exposure; finite polymer-size effects; line collapsing; lithography on topography**			**Meso-scale resist models with finite molecule effects; resist flare**		**Non-conventional photoresist models and coupling with etch models**
	Full-chip lithography simulation	**Simulation of lithography across whole chip to detect weak spots**		**Simulation of lithography and etching across whole exposure field to detect weak spots**						
	Front End Process Modeling									
WAS	Gate stack*	**◆ High-κ dielectrics and gate materials (interfaces, impurity diffusion, electrical barrier) [4]**		**Model material properties and electrical behavior of prioritized alternative dielectrics and gates (interfaces, defects, impurities, mobility, leakage) [5]**					**Modeling of new process steps / processing and properties of alternative materials**	
IS	Gate stack*	**◆ High-κ dielectrics and gate materials (interfaces, impurity diffusion, electrical barrier) [4]**			**Model material properties and electrical behavior of prioritized alternative dielectrics and gates (interfaces, defects, impurities, mobility, leakage - incl. metal gates and FUSI) [5]**				**Modeling of new process steps / processing and properties of alternative materials**	

Table 123a Modeling and Simulation Technology Requirements: Capabilities—Near-term Years UPDATED (continued)

**For 2005/2006, interim solutions are known but research is still needed towards mature commercial solutions.*

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
WAS	Diffusion and activation models	Interface influences and activation for ultra-shallow junction formation		Enhancements of models for Si, extension for Si based materials incl. stress/strain and new annealing steps (e.g. flash/laser anneals, SPER). Atomistic modeling to complement experiments and continuum models.						
IS	Diffusion and activation models	Interface influences and activation for ultra-shallow junction formation		Enhancements of models for Si, extension for Si based materials incl. stress/strain and new annealing steps (e.g. flash/laser anneals, SPER)			Atomistic modeling to complement experiments and continuum models.			
	Topography and Material Modeling [6]									
WAS	Deposition	Integration between feature scale and equipment simulations		Electrical properties and stress incl. microstructure; layout dependence; prediction of liquid dispense (resist, spin-on ULK) on planarity and gate pattern; coupling with etching, lithography and CMP models		Adhesion and reliability, including microstructure; full molecular dynamics (or atomistic) feature scale models, prediction of surface properties				
IS	Deposition	Integration between feature scale and equipment simulations		Electrical properties and stress incl. microstructure; layout dependence				Prediction of microstructure and surface properties		
WAS	Planarization *	◆ Comprehensive 3D physical CMP models			Chip-level including dummy placement optimization, padwear and conditioning disc modeling, physics based optimization of rates, uniformity, and defect reduction		CMP process for circuit design including process variations			
IS	Planarization *	~~Comprehensive~~ Physical CMP models incl. dummy placement optimization			Chip-level ~~including dummy placement optimization, padwear and conditioning disc modeling,~~ physics based optimization of rates, uniformity~~, and defect reduction~~		Simulation of defect reduction incl. padwear and condition disc modeling			
WAS	Etching	(Surface) physics based feature scale models (incl. redeposition)	Integration of feature-scale simulation with equipment (plasma) models; process integration (coupling of etch-deposition-plating-CMP-lithography- including data beyond topography to also include sub-surface material property prediction), full molecular dynamlcs (or atomistic) feature scale models							
IS	Etching	(Surface) physics based feature scale models (incl. redeposition)		Integration of feature-scale simulation with equipment (plasma) models; process integration (coupling of etch-deposition-plating-CMP-lithography) ~~including data beyond topography to also include sub-surface material property prediction), full molecular dynamlcs (or atomistic) feature scale models~~				Including data beyond topography to also include sub-surface material property prediction), full molecular dynamics (or atomistic) feature scale models		

Table 123a Modeling and Simulation Technology Requirements: Capabilities—Near-term Years UPDATED (continued)

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
WAS	Alternative material modeling				**Calculation of thermal (thermodynamic), mechanical and electronic properties; process impact on intrinsic material behavior, integrity and electrical performance under strain**					
IS	Alternative material modeling			**Calculation of thermodynamic and electronic properties**	**Calculation of ~~thermal (thermodynamic),~~ mechanical ~~and electronic~~ properties; process impact on intrinsic material behavior, integrity and electrical performance under strain**					
	Equipment impact on process results including material properties			-			**Computer engineered materials and process recipes; predictive manufacturability and yield; full process integration models. Integrated equipment/feature scale modeling extended to include material information from the atomic scale**			
	Numerical Device Modeling [7]									
WAS	Transport modeling [8],	**Mobility models incl. stress, surface roughness effects of nitrided oxides and orientation of the channel**		**Mobility models for high-κ materials**		**Efficient inclusion of quasi-ballistic transport**				
IS	Transport modeling [8]	**Mobility models incl. stress, surface roughness effects of nitrided oxides and orientation of the channel**		**Mobility models for high-κ materials; efficient inclusion of quasi-ballistic transport**			**QM confinement in thin films (esp. SOI)**			
WAS	Additional requirements for non-classical CMOS	**Device models to include additional interfaces (esp. with respect to mobility in thin films)**		**Efficient quantum-mechanical simulation of 3D device structures, including thin films, consistent with mobility models**					**Nanoscale simulation capability including accurate atomistic and quantum effects**	
IS	Additional requirements for non-classical CMOS	**Device models to include additional interfaces (esp. with respect to mobility in thin films)**		**Efficient quantum-mechanical simulation of 3D device structures, including thin films, consistent with mobility models**					**Nanoscale simulation capability including accurate atomistic and quantum effects; QM confinement in nanowires etc**	
WAS	Novel memory devices	**Material properties and device modeling of MRAMs, PCMs, FeRAMs and SONOS/NROMs**								
IS	Novel memory devices *	**◆ Unit-cell performance modeling of MRAMs, PCMs, FeRAMs and SONOS/NROMs**			**Material properties and reliability modeling of novel memory devices**					
WAS	RF modeling *	**◆ Physical device models for HF noise and mobility in III/Vs**								
IS	RF and noise modeling *	**◆ Physical device models for HF noise and mobility in III/Vs**								
	Circuit Component Modeling [9]									
WAS	Active devices*	**◆ Non-classical CMOS compact models / non-quasi-static models and series resistance**		**Circuit models for non-classical CMOS devices including reliability and influences of statistics**		**Include ballistic effects**			**Circuit models for nanoscale devices and interconnects**	
IS	Active devices*	**◆ Non-classical CMOS compact models / non-quasi-static models and series resistance**		**Circuit models for non-classical CMOS devices including reliability and influences of statistics**		**Include quasi-ballistic effects and non-stationary transport**			**Circuit models for nanoscale devices and interconnects**	

Table 123a Modeling and Simulation Technology Requirements: Capabilities—Near-term Years UPDATED (continued)

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
WAS	Interconnects and integrated passives	**Hierarchical full chip RLC [10]**		**Hierarchical process-aware full-chip RLC**		**Include self-heating and reliability**			**Mixed electrical/optical simulation**	
IS	Interconnects and integrated passives	**Hierarchical full chip RLC [10]**		**Hierarchical process-aware full-chip RLC**		**Include self-healing and reliability**			**Mixed electrical/optical simulation**	
	Process and materials impact on electrical performance of interconnects *	**◆ Models that relate material properties (process related or fundamental) to electron transport (e.g. in conducting lines). Includes models for electron scattering. Models that predict paths to material property repair (e.g. low-κ repair, capacitance repair)**								
	Package Modeling									
WAS	Electrical modeling*	**◆ Unified RLC extraction for package/ chips**	**Reduced order models**		**Full-wave analysis**		**Mixed electrical/optical analysis**			
IS	Electrical modeling*	**◆ Unified RLC extraction and multiscale modeling for package / chips**		**Reduced order models**		**Full-wave analysis**		**Mixed electrical/optical analysis**		
WAS	Thermal-mechanical modeling *	**◆ Thermo-mechani-cal-integrated models**	**Include non-bulk and porous materials properties**	**Include reliability (esp. life prediction)**						
IS	Thermal-mechanical modeling *	**◆Thermo-mechani-cal-integrated models**	**◆ Include non-bulk and porous/air gap materials properties**	**Include reliability (esp. life prediction)**						
WAS	Material properties *	**◆ Improved material models (visco-elasticity, creep, plasticity), interfaces**	**Full die simulation**							
IS	Material properties *	**◆ Improved material models (visco-elasticity, creep, plasticity), interfaces**		**Full die simulation**						
	Numerical analysis									
WAS	Meshing *	**◆ Robust, reliable grid generation including moving boundaries**								
IS	Meshing *	**◆ Robust, reliable 3D grid generation including moving boundaries**								
	Algorithms	**More robust and more parallelizable algorithms**			**Discretization schemes alternative e.g. to box methods**		**Efficient atomistic/quantum methods; ab-initio or molecular dynamics based topography simulations**			

Notes for Table 123a&b: UPDATED [Numbering of notes]

[1] Standard lens/resist

[2] Other final lens

[3] Other lens + other resist

[4] Models that at least roughly predict effects like oxygen vacancies and Hf-Si interface states are required, as those effects cause flatband shifts and fermi-level pinning. Currently there are no commercial tools available in a typical TCAD environment. Thus very phenomenological, a posteriori approaches are used. They are limited also to only some effects and by using models that were originally not designed for those effects.

[5] "Alternative" refers to materials so far not prioritized in PIDS

[6] Emphasis in topography steps shifted to material aspects towards long-term years

[7] In Numerical Device Modeling equations are solved that are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect to spatial coordinates) are employed. The goal is technology optimization and device insight.

[8] This row includes all aspects important for all devices, that is, especially classical CMOS bulk devices

[9] In Circuit Element Modeling no spatially resolved models are used. Approximately analytically solveable, physically based models give guidance for the used relations between electrical quantities. The goal is a description of device behavior (currents, charges, noise) in circuit simulators

[10] This refers to a minimum of functional sub-circuits

Table 123b Modeling and Simulation Technology Requirements: Capabilities—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	Lithography							
WAS	Exposure	NGL models and modeling of materials and components (immersion, EUV, EPL, ML2 lithographic processes, imprint)						
IS	Exposure	NGL models and modeling of materials and components (immersion, EUV, ~~EPL,~~ ML2 lithographic processes, imprint)						
WAS	Resist models	Non-conventional photo-resist models and coupling with etch models						
IS	Resist models	Models for non-conventional photo-resists and coupling with etch models						
	Front End Process Modeling							
	Gate Stack*	Modeling of new process steps / processing and properties of alternative materials						
	Diffusion and activation models	New technology needed						
	Topography and Material Modeling							
WAS	Alternative material modeling	Calculation of thermal (thermo-dynamic), mechani-cal and electronic properties; process impact on intrinsic material behavior integrity and electrical performance under strain	Atomistic material model					
IS	Alternative material modeling	Atomistic material model						
	Equipment impact on process results including material properties	Computer engineered materials and process recipes; predictive manufacturability and yield; full process integration models. Integrated equipment/feature scale modeling extended to include material information from the atomic scale						
	Numerical Device Modeling [7]							
	Additional requirements for non-classical CMOS	Nanoscale simulation capability including accurate atomistic and quantum effects						
ADD	Additional requirements for devices beyond non-classical CMOS	Nanoscale simulation capability including accurate atomistic and quantum effects for ERD devices						
	Circuit Component Modeling [9]							
	Active devices*	Circuit models for nanoscale devices and interconnects						
	Interconnects and integrated passives	Mixed electrical/optical simulation		Reliability prediction in coupled modeling				
	Package Modeling							
	Electrical modeling*	Reliability prediction in coupled modeling						
	Numerical analysis							
	Algorithms*	Multi-scale simulation (atomistic-continuum); fast coupling of equipment-topography-electrical-reliability models; hierarchical full-chip simulation						

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

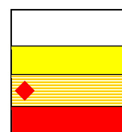

Table 124 Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term Years
UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
WAS	*Technology-development cost reduction (due to TCAD)*	35%	40%	40%	40%	40%	40%	40%	40%	40%
IS	*Technology development costs reduction potential if TCAD is appropriately used [1]*	35%	40%	40%	40%	40%	40%	40%	40%	40%
	Lithography Modeling									
WAS	CD prediction accuracy (incl. OP effects) for dense and isolated lines – *3% of MPU physical gate length*	0.9 nm	0.8 nm	0.7 nm	0.7 nm	0.6 nm	0.5 nm	0.5 nm	0.4 nm	0.4 nm
IS	**Absolute** CD prediction accuracy (incl. OP effects) for dense and isolated lines **– % of actual CD (=printed gate length) [2]**	3%	3%	3%	3%	3%	3%	3%	3%	3%
ADD	**Accuracy of sensitivity of CD vs. relevant technology parameters (dose, defocus, pitch, ….) [3]**	10%	10%	10%	10%	10%	10%	10%	10%	10%
	Front End Process Modeling									
	Vertical junction depth simulation accuracy (% of physical gate length)	10% (3.2 nm)	10% (2.8 nm)	10% (2.5 nm)	10% (2.2 nm)	10% (2.0 nm)	10% (1.8 nm)	10% (1.6 nm)	10% (1.4 nm)	10% (1.3 nm)
WAS	Lateral junction depth: 50% of FEP Lgate 3 sigma	1.9 nm	1.7 nm	1.5 nm	1.3 nm	1.2 nm	1.1 nm	1.0 nm	0.9 nm	0.8 nm
IS	Lateral junction depth **simulation accuracy**: (% of physical gate length)	5%	5%	5%	5%	5%	5%	5%	5%	5%
ADD	Accuracy of sensitivity of junction depth with respect to implantation and anneal conditions [3]	5%	5%	5%	5%	5%	5%	5%	5%	5%
WAS	Total source/drain series resistance (accuracy)	10%	10%	10%	10%	10%	10%	10%	10%	10%
IS	Total source/drain series resistance (accuracy of activation)	10%	10%	10%	10%	10%	10%	10%	10%	10%
	Topography Modeling									
WAS	General etch cross wafer uniformity (% accuracy of etch depth)	10.0%	10.0%	10.0%	10.0%	10.0%	10.0%	10.0%	10.0%	10.0%
WAS	Etch cross wafer uniformity of STI depth (% accuracy of STI depth)	3.0% (11.0 nm)	3.0% (10.8 nm)	3.0% (10.6 nm)	3.0% (10.2 nm)	3.0% (10.1 nm)	3.0% (9.9 nm)	3.0% (9.7 nm)	3.0% (9.5 nm)	3.0% (9.4 nm)
WAS	General deposition cross wafer uniformity (% accuracy of film thickness)	5%	5%	5%	5%	5%	5%	5%	5%	5%
IS	Wafer scale deposition/etching/CMP accuracy [4]	5%	5%	5%	5%	5%	5%	5%	5%	5%
DELETE	~~High κ film deposition cross wafer uniformity (% accuracy of film thickness)~~	~~2.0%~~	~~2.0%~~	~~2.0%~~	~~2.0%~~	~~2.0%~~	~~2.0%~~	~~2.0%~~	~~2.0%~~	~~2.0%~~
WAS	General 2D/3D topography accuracy (% accuracy of the DRAM 1/2 pitch)	5% (4 nm)	5% (3.5 nm)	5% (3.3 nm)	5% (2.9 nm)	5% (2.5 nm)	5% (2.3 nm)	5% (2.0 nm)	5% (1.8 nm)	5% (1.6 nm)
IS	General 2D/3D topography accuracy (% accuracy of **feature dimensions**)	5%	5%	5%	5%	5%	5%	5%	5%	5%

Table 124 Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term Years
UPDATED (continued)

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
	Gate 2D/3D topography accuracy (% accuracy of the MPU physical gate length)	**1.8%**	**1.8%**	**1.8%**	**1.8%**	**1.8%**	**1.8%**	**1.8%**	**1.8%**	**1.8%**
		(0.58 nm)	**(0.50 nm)**	**(0.45 nm)**	**(0.40 nm)**	**(0.36 nm)**	**(0.32 nm)**	**(0.29 nm)**	**(0.25 nm)**	**(0.23 nm)**
	Gate sidewall spacer 2D/3D topography accuracy (% accuracy of sidewall width)	**5.0%**	**5.0%**	**5.0%**	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**
		(1.8 nm)	**(1.5 nm)**	**(1.4 nm)**	**NA**	**NA**	**NA**	**NA**	**NA**	**NA**
	Interconnect 2D/3D topography accuracy (% accuracy of MPU/ASIC Metal 1 (M1) ½ Pitch	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**
		(4.5 nm)	**(3.9 nm)**	**(3.4 nm)**	**(3.0 nm)**	**(2.6 nm)**	**(2.3 nm)**	**(2.0 nm)**	**(1.8 nm)**	**(1.6 nm)**
	Numerical Device Modeling [5]									
WAS	Accuracy of ft and fmax at given ft (% of maximum chip frequency)	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**
IS	Accuracy of ft and fmax ~~at given ft (% of maximum chip frequency~~)	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**
WAS	Gate leakage accuracy (% of Ig)	**25%**	**25%**	**25%**	**25%**	**25%**	**25%**	**25%**	**25%**	**25%**
IS	**Gate leakage accuracy (% of Ig) [6]**	**25%**	**25%**	**25%**	**25%**	**25%**	**25%**	**25%**	**25%**	**25%**
	Ion accuracy	**5%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
WAS	Ioff accuracy	**30%**	**30%**	**30%**	**30%**	**30%**	**30%**	**30%**	**30%**	**30%**
IS	Leakage current accuracy incl. S/D gate leakage and band-to band tunneling ~~Ioff accuracy~~	**30%**	**30%**	**30%**	**30%**	**30%**	**30%**	**30%**	**30%**	**30%**
DELETE	~~Long-channel Vt accuracy [7]~~	~~**3%**~~	~~**3%**~~	~~**3%**~~	~~**3%**~~	~~**3%**~~	~~**3%**~~	~~**3%**~~	~~**3%**~~	~~**3%**~~
WAS	Vt rolloff accuracy (mV) [8]	**15 mV**	**10 mV**	**10 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**
IS	Length-dependent Vt ~~rolloff~~ accuracy (mV) [9]	**15 mV**	**10 mV**	**10 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**
ADD	**Width-dependent Vt ~~rolloff~~ accuracy (mV) [10]**	**15 mV**	**10 mV**	**10 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**	**7 mV**
ADD	**Accuracy of Gm and Gd at Vt +150mV versus L, Vbs, Vds and T**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**
	Circuit Element Modeling/ECAD [11]									
	I-V error in saturation region	**8%**	**6%**	**6%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**
	I-V error in saturation region	**8%**	**6%**	**6%**	**5%**	**5%**	**5%**	**5%**	**5%**	**5%**
	I-V error in linear region	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
WAS	I-V error in subthreshold and off-current	**15%**	**15%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**
IS	Leakage current incl. I_{off} and gate current accuracy.	**15%**	**15%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**	**10%**

Table 124 Modeling and Simulation Technology Requirements: Accuracy and Speed—Near-term Years UPDATED (continued)

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm) (contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
WAS	Intrinsic MOS C-V accuracy	5%	5%	5%	5%	5%	5%	5%	5%	5%
IS	Intrinsic MOS C-V accuracy	5%	5%	5%	5%	5%	5%	5%	5%	5%
	Parasitic C-V accuracy	5%	5%	5%	5%	5%	5%	5%	5%	5%
WAS	Accuracy of Gm and Gd at Vt +150mV versus L, Vbs, Vds and T	10%	10%	10%	10%	10%	10%	10%	10%	10%
IS	Accuracy of Gm and Gd at Vt +150mV versus L, Vbs, Vds and T	10%	10%	10%	10%	10%	10%	10%	10%	10%
WAS	Circuit delay accuracy (% of 1/maximum chip frequency)	5%	5%	5%	5%	5%	5%	5%	5%	5%
IS	Circuit delay accuracy (% of 1/maximum chip frequency)	5%	5%	5%	5%	5%	5%	5%	5%	5%
DELETE	~~RLC delay accuracy (% of 1/maximum chip frequency)~~	~~5%~~	~~5%~~	~~5%~~	~~5%~~	~~5%~~	~~5%~~	~~5%~~	~~5%~~	~~5%~~
	Package Modeling									
	Package delay accuracy (% of 1/off-chip clock frequency)	1%	1%	1%	1%	1%	1%	1%	1%	1%
WAS	Temperature distribution for package (accuracy)	1C	1C	1C	1C	1C	1C	1C	1C	1C
IS	Temperature distribution for package (accuracy)	3%	3%	3%	3%	3%	3%	3%	3%	3%
DELETE	~~*Numerical Method*~~									
DELETE	~~Speed-up of algorithms for 3D process/device/interconnect simulation (compared with year 2000)*~~	~~8×~~	~~11.2×~~	~~16×~~	~~22.4×~~	~~32×~~	~~45x~~	~~64x~~	~~90x~~	~~128x~~

Table 124a notes: UPDATED

[1] This line does not give a quantitative assessment of the industrial requirement but gives the average of estimates obtained from companies on cost reductions in best practice cases through use of TCAD in development
[2] CD averaged - LER not included. After calibration of resist parameters
[3] Influence of process parameters on CD, etc. should be predicted with that maximum relative error
[4] For gate oxide this means atomistic precision
[5] In Numerical Device Modeling equations are solved which are typically based on fundamental physics and describe the electrical behavior on spatially fine resolved quantities. This means usually partial differential equations (with respect spatial coordinates) are employed. The goal is technology optimization and device insight
[6] Not including effects of high-k / metal gate
[7] Absolute values strongly differ for HP and LSTP. Important aspects for nominal devices also included in rolloff accuracy
[8] (Positive) difference in Vth of nominal and subnominal device
[9] Difference between simulated and measured Vth for different channel lengths
[10] Difference between simulated and measured Vth for different channel width
[11] In Circuit Element Modeling no spatially resolved models are used. Approximately analytically solveable, physically based models give guidance for the used relations between electrical quantities. The goal is a description of device behavior (currents, charges, noise) in circuit simulators.

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known