



# NAND Flash Architecture and Specification Trends

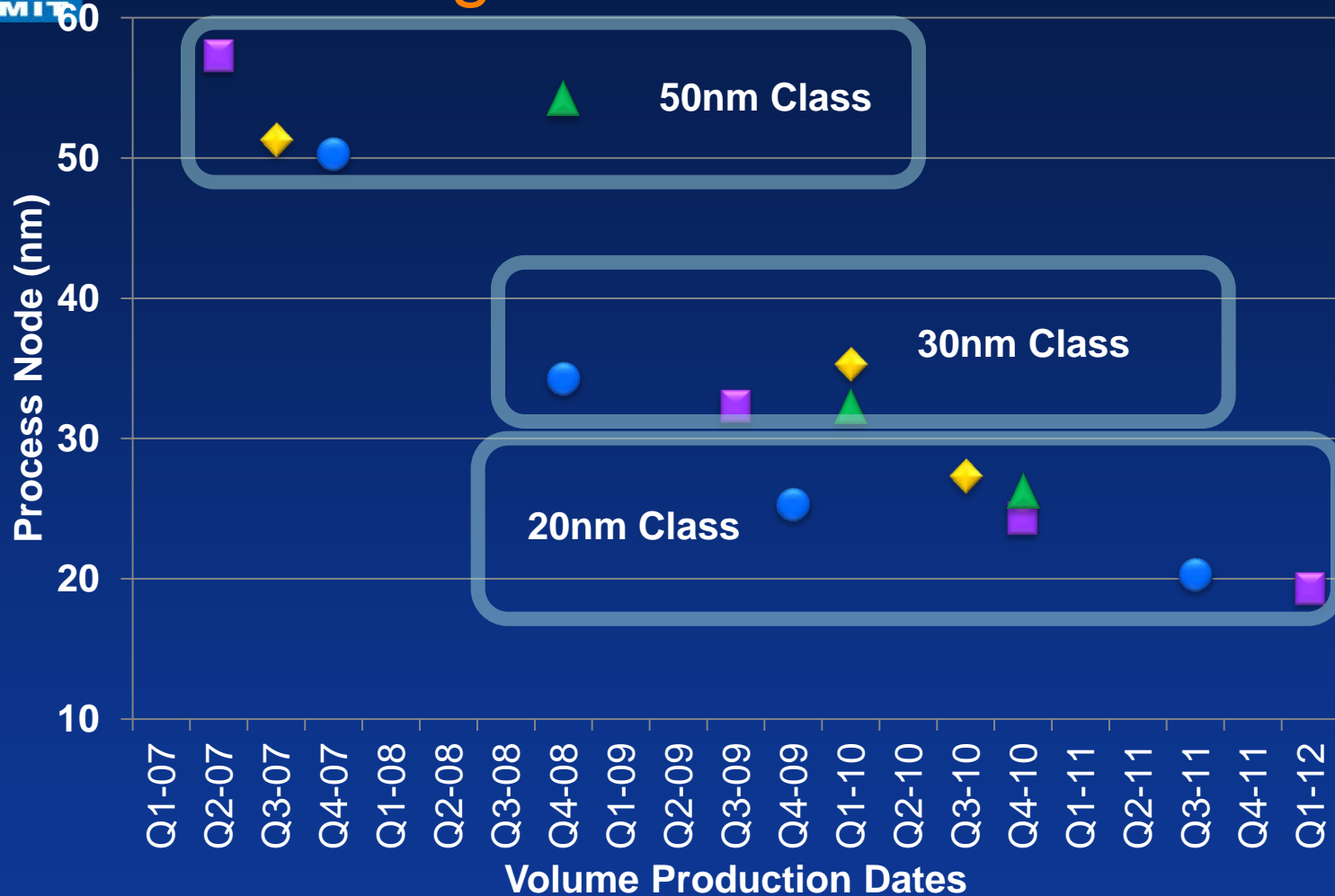
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The logo for the Flash Memory Summit features a stylized yellow sunburst with multiple rays. Below the sunburst, the word "Flash" is written in red, "Memory" in blue, and "SUMMIT" in white on a blue rectangular background.

# Flash Memory Summit Topics

- NAND Flash trends
- SSD/Enterprise application requirements
- A look to the future

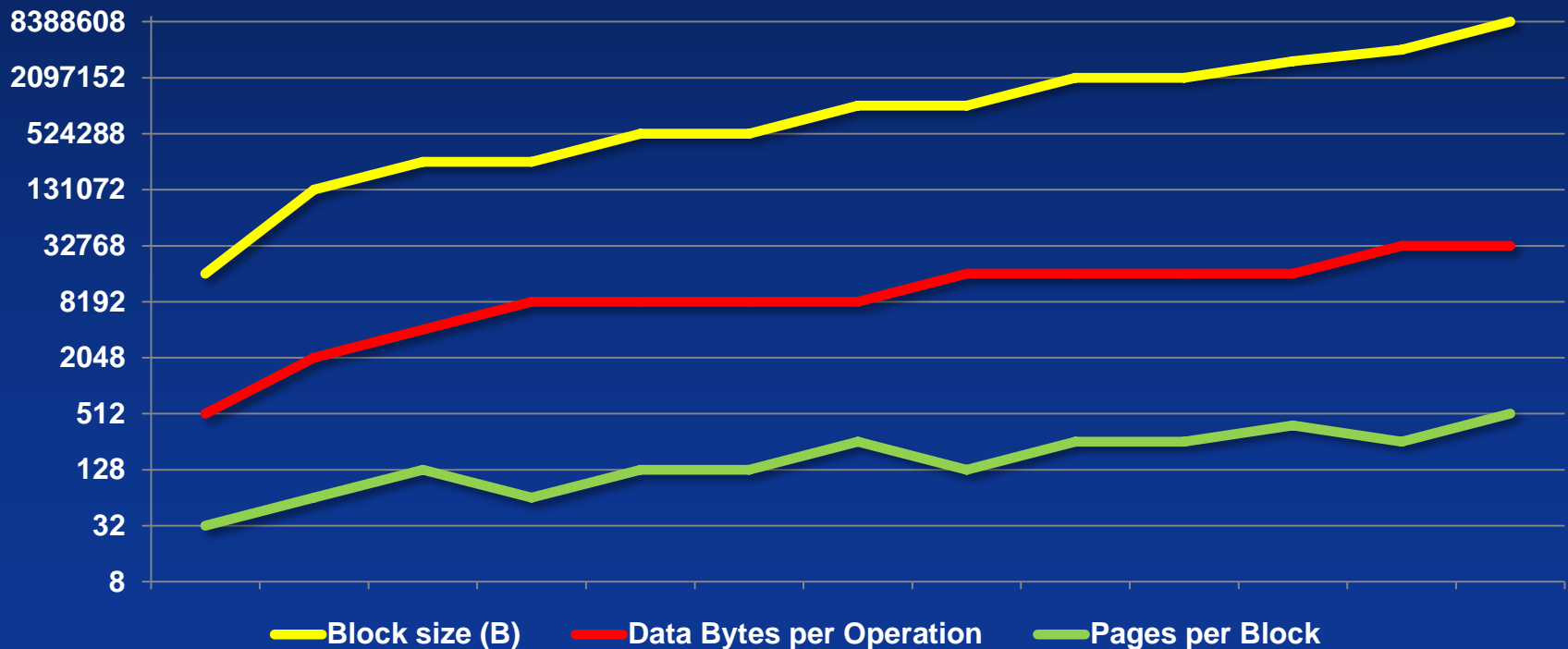
# NAND Process Migration: Shrinking Faster than Moore's Law



● Company A    ◆ Company B    ■ Company C    ▲ Company D

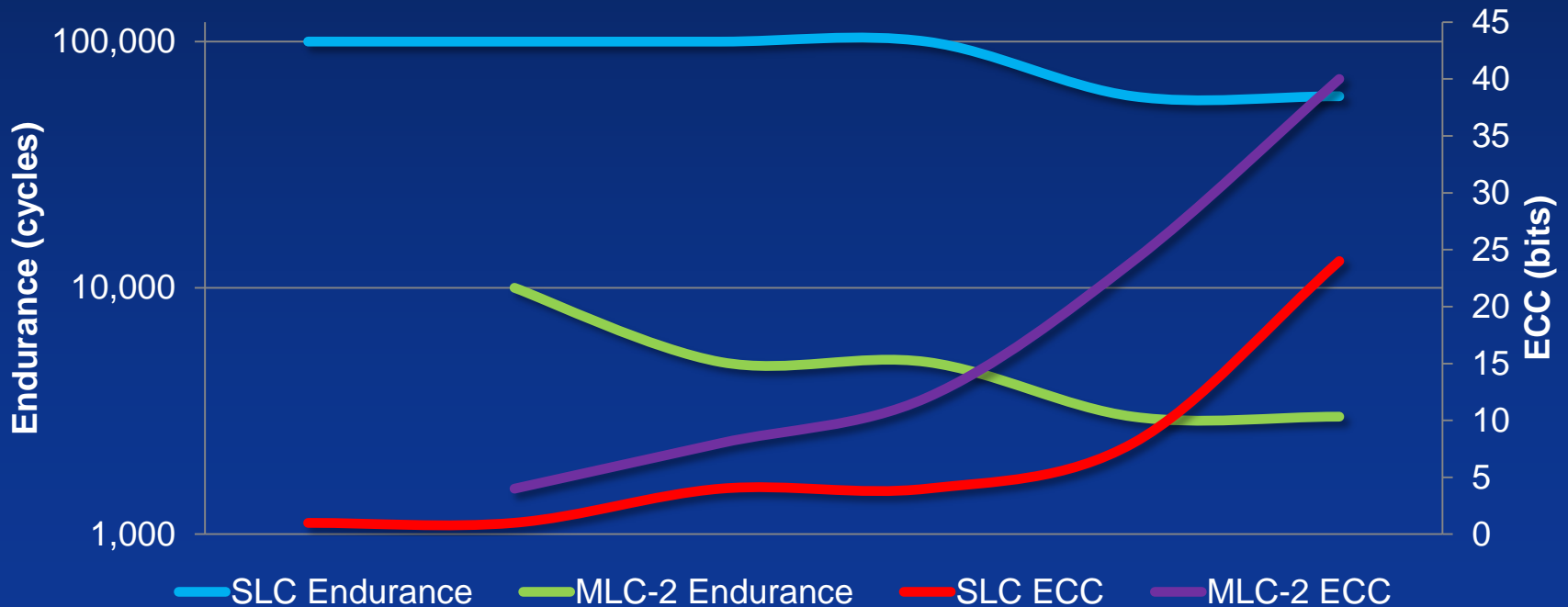
# Memory Organization Trends

- NAND block size is increasing
  - Larger page sizes and more planes increase sequential throughput
  - More pages per block reduce die size



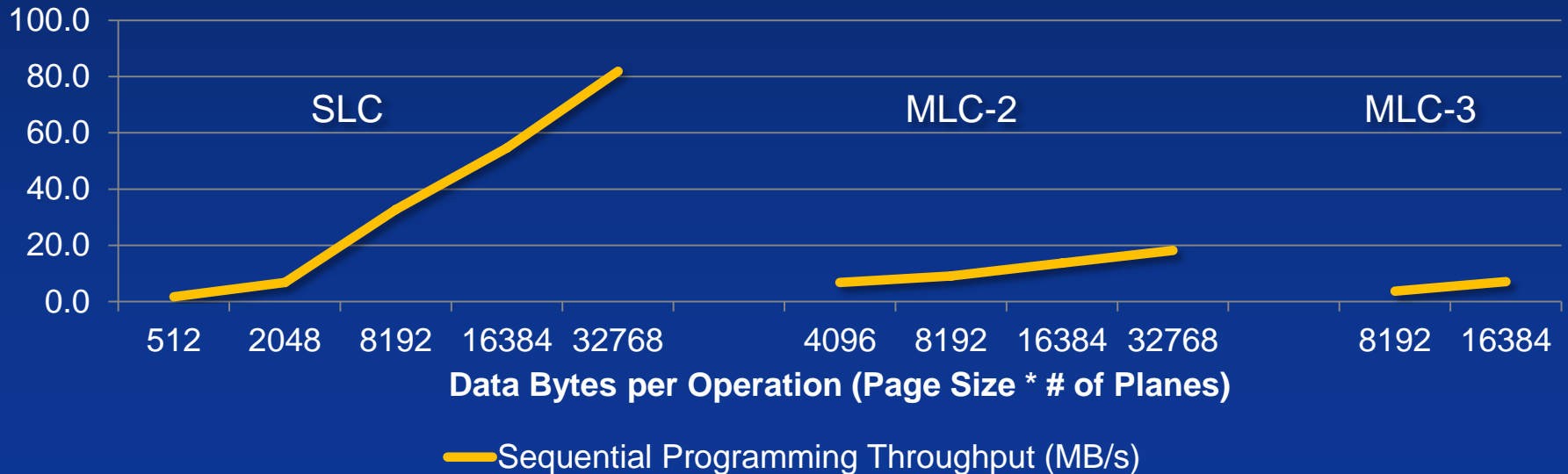
# Consumer-Grade NAND Flash: Endurance and ECC Trends

- Process shrinks lead to fewer electrons per floating gate
- ECC used to improve data retention and endurance
- To adjust for increasing RBERs, ECC is increasing exponentially to achieve equivalent UBERs



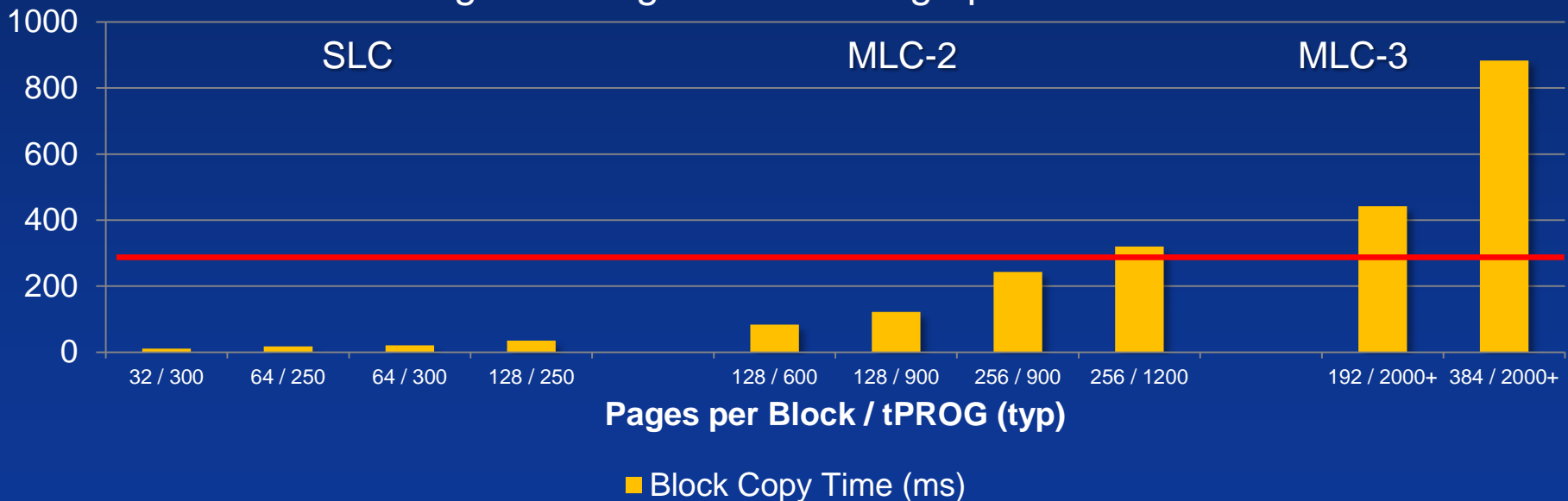
# Larger Page Sizes Improve Sequential Write Performance

- For a fixed page size, write throughput decreases as NAND process shrinks
- NAND vendors increase the page size to compensate for slowing array performance
- Write throughput decreases with more bits per cell



# More Pages Per Block Affect Random Write Performance

- The block copy time is the largest limiting factor for random write performance
- As block copy time increases, random performance decreases
  - Number of pages per block is the dominant factor
  - Increase of  $t_{\text{PROG}}$  is the next largest factor
  - Increase in I/O transfer time due to increasing page size (effect not shown below) is also a factor
- Some card interfaces have write timeout specs at 250ms, which means that block management algorithms manage partial blocks



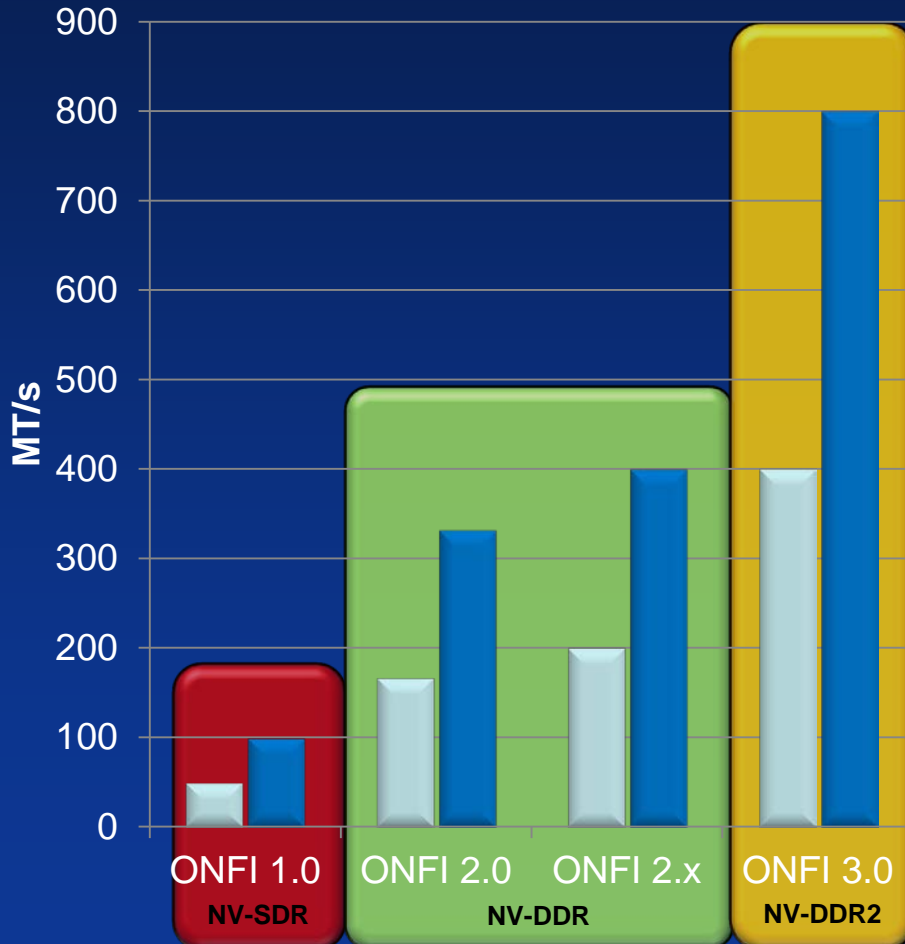
# NAND Interface Trends

Interface Standard (x8)	Max Throughput (MT/s)
No standard	40
ONFI 1.0 NV-SDR (12/06)	50
ONFI 2.0 NV-DDR (2/08)	133
ONFI 2.1-2.3 NV-DDR (1/09, 9/09, 8/10)	200
Toggle Mode (not yet published)	200
ONFI 3.0 NV-DDR2 (3/11)	400
Toggle Mode 2 (not yet published)	400



# The ONFI Advantage

■ Single Channel Package ■ Dual Channel Package



- Supports simultaneous READ, PROGRAM, and ERASE operations on multiple die on the same chip enable since ONFI 1.0
- Only industrystandard NAND interface capable of 400 MT/sec data rate from a single die
- Two independent channels in a single package (doubles the I/O bandwidth)
- ONFI 3.0 published and available at [onfi.org](http://onfi.org)



# SSD/Enterprise vs. Consumer Applications

- SSD/Enterprise applications are different than typical consumer applications in several ways
  - Higher total system density
  - More throughput required, including in random operations
  - Fixed data sizes—for example, database: 4KB or 8KB
  - Higher endurance/reliability requirements
  - More consistent use over time
  - Power within budget for parallel operations



# Meeting SSD/Enterprise Application Requirements

<b>Application Requirement</b>	<b>Controller</b>	<b>SSD/EnterpriseGrade NAND Flash</b>
Higher system density	Ability to handle many NAND Flash—some controllers up to 256 die	Lower DPM
More throughput	Page-based block management, DRAM cache, Overprovisioning, More I/O channels, Faster I/O channels, Multiple ECC engines, Simultaneous operations	Faster I/O channel



# Meeting SSD/Enterprise Application Requirements, Part 2

<b>Application Requirement</b>	<b>Controller</b>	<b>SSD/Enterprise-grade NAND Flash</b>
Higher endurance / reliability	Higher ECC	More ECC required, Lower UBER, More endurance
More consistent use over time	Balanced block management to reduce write amplification	
Power within budget for parallel operations	Block management throttles parallelism as needed	Peak power reduction

- Higher endurance: achieves higher endurance than consumer-grade NAND Flash
- Lower data retention at max endurance
  - No change to data retention at time 0
  - Enterprise applications tend to use NAND more consistently over its lifetime, so data retention *at max cycling* becomes less important and is reduced



# SSD/EnterpriseGrade NAND Flash, Part 2

- ECC tuned for lower UBER
  - Providing more ECC to a consumergrade NAND Flash does not necessarily improve endurance
  - SSD/Enterprisegrade NAND Flash is tuned to improve endurance while reducing UBER, requiring more ECC
- Modest performance
  - NAND array performance is modestly slower than consumergrade NAND Flash
  - Controller helps achieve better system throughput through more channels, faster interface speeds, overprovisioning, higher parallelism



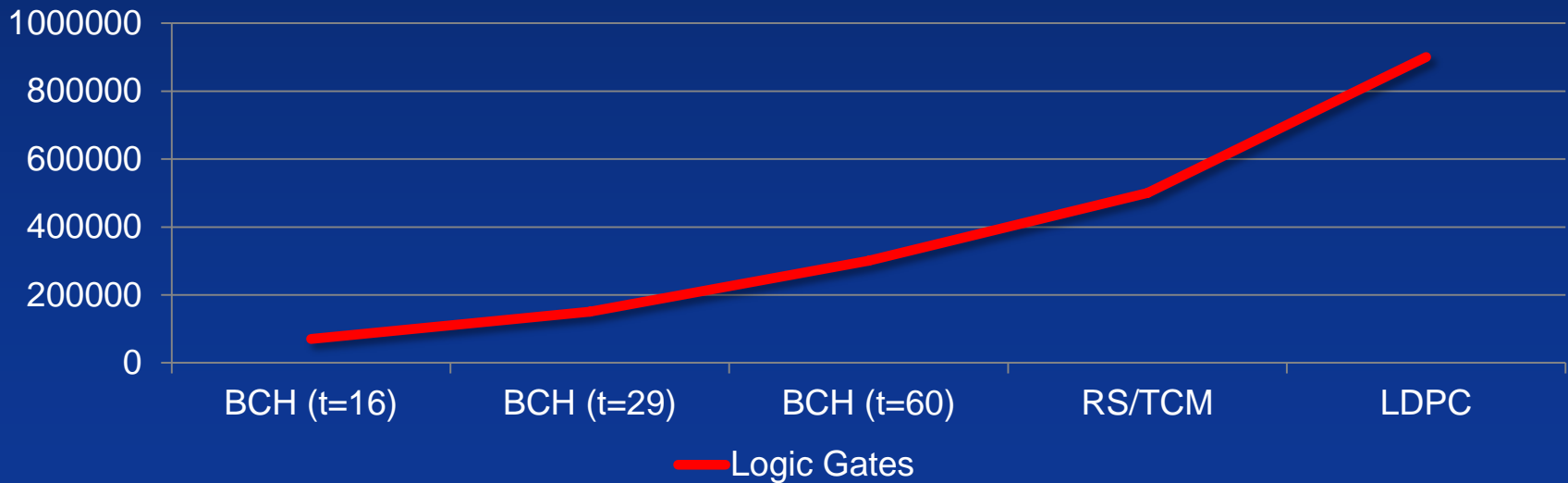
# SSD/EnterpriseGrade NAND Flash, Part 3

- Fast I/O interface
  - Allows better utilization of I/O channels—higher bandwidth
  - Immediately useful for single die read performance
  - Modest improvement for write performance with multiple die
  - Reduces I/O channels required on controller
  - Support 200 MB/s today with 400 MB/s coming

# Look to the (Near) Future

- ECC is going to continue to increase to the point that it will be a significant amount of real estate on a multichannel controller

Logic Gates

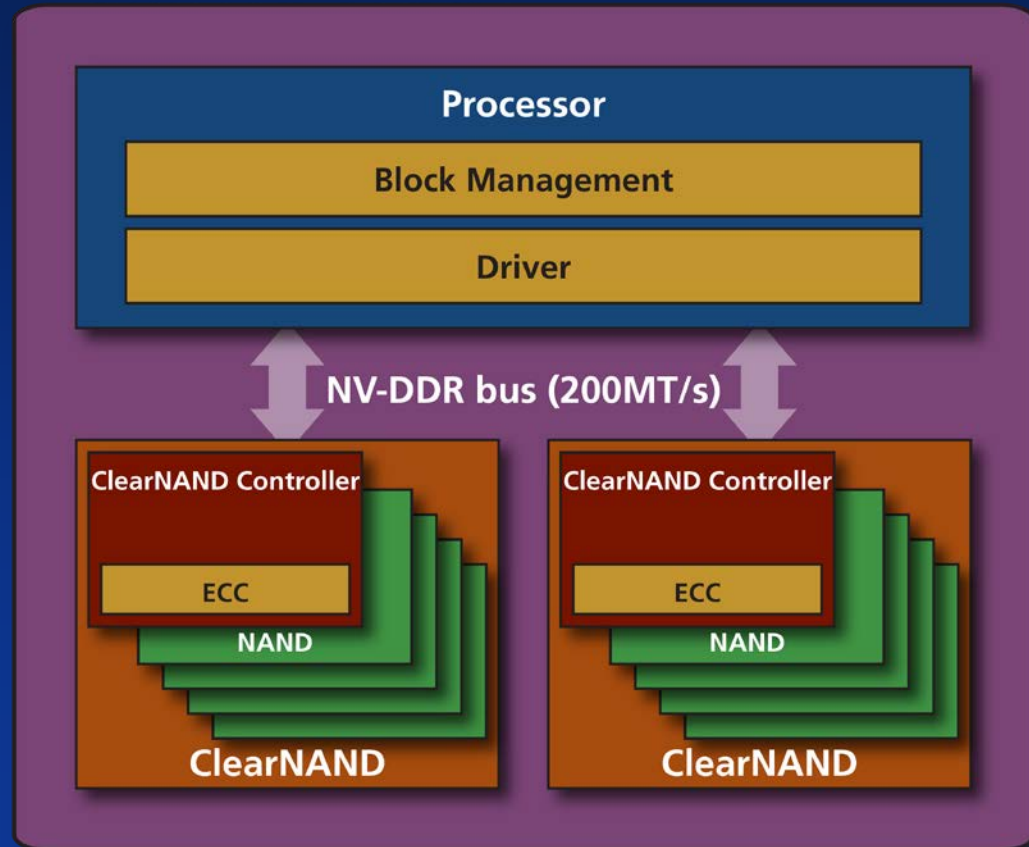




# How to Handle Increasing ECC?

- ECC is technology dependent and typically requires a new controller to support higher levels
- Block management and drivers aren't technology dependent and can be updated in software/firmware
- Solution: Move ECC to the NAND package and tightly coupled to the underlying NAND technology
- Also covers NAND aggregation, reducing channel loading
- Other benefits
  - In package data copying
  - Volume addressing allows multiple CE#s to be combined into one
- For more benefits, see "System Benefits of EZNAND/Enhanced ClearNAND Flash" by Carla Lay in Session 305 on Thursday at 9:50 AM

## ClearNAND Solution





# Questions?

Revisit the Micron FMS presentations at [www.micron.com/fms](http://www.micron.com/fms)

## About Michael Abraham

- Architect in the NAND Solutions Group at Micron
- Covers advanced NAND and PCM interfaces and system solutions
- BS degree in Computer Engineering from Brigham Young University



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