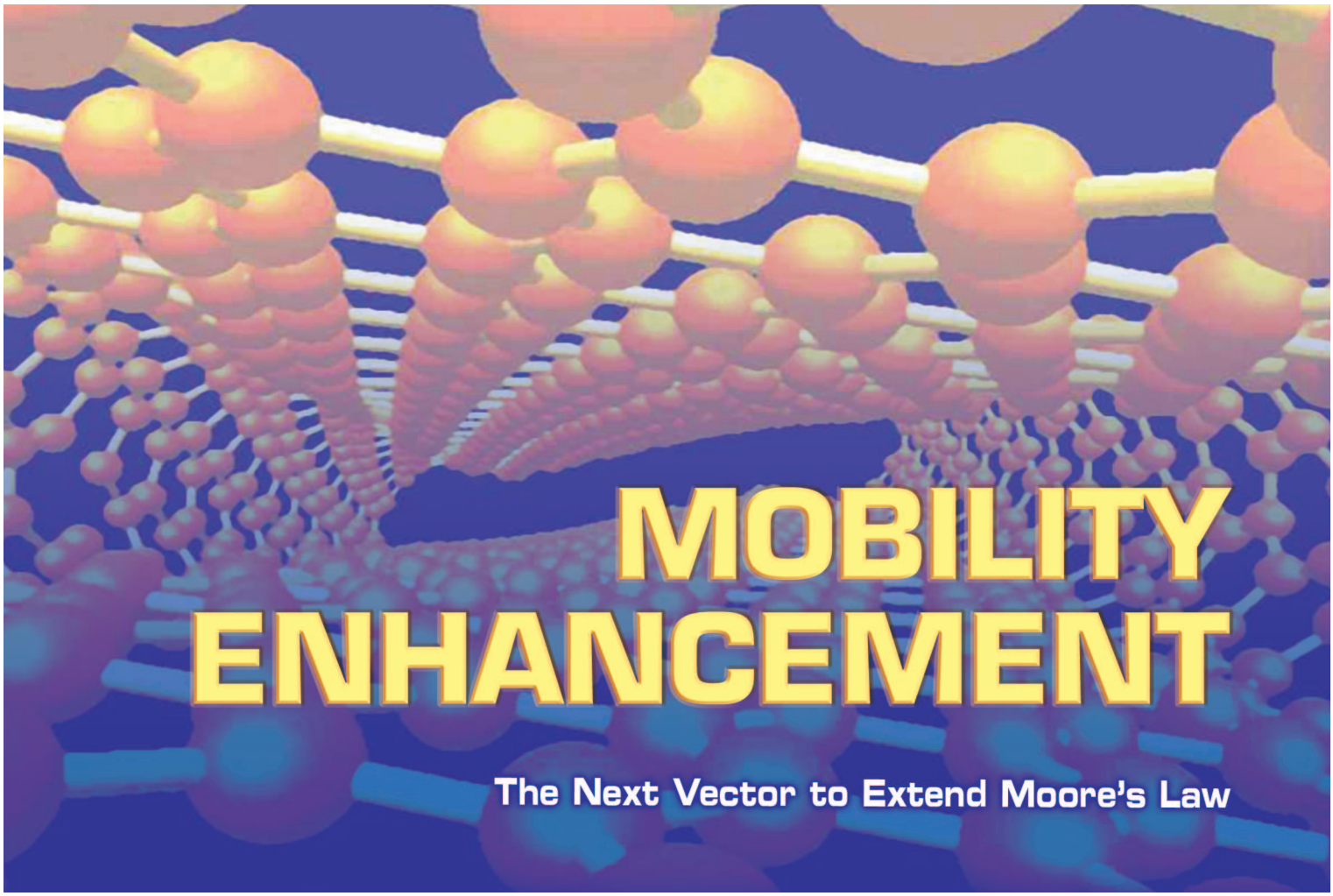

MOBILITY ENHANCEMENT

The Next Vector to Extend Moore's Law

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For the past four decades, geometric scaling of silicon (Si) complementary metal-oxide semiconductor (CMOS) transistors has enabled not only an exponential increase in circuit integration density (Moore's law), but also a corresponding enhancement in the transistor performance itself. Simple metal-oxide semiconductor field-effect transistor (MOSFET) geometric scaling has driven the industry to date. But as the transistor gate length drops to 35 nm [1]–[3] and the gate oxide thickness drops to ~1 nm, physical limitations, such as off-state leakage current and power density, make geometric scaling an increasingly challenging task. To continue CMOS device historical performance improvement, the industry needs a new scaling vector. Starting with the 90-nm technology generation, mobility enhancement through uniaxial process-induced strained Si has emerged as the next scaling vector being widely adopted in logic technologies [1], [3], [4].

This article is targeted as an introduction to the physics of strained Si and the current state of the art in uniaxial strained Si MOSFET. The first part of the article explains how strain alters the valence and conduction band of Si as well as scattering rates. This is followed by a review of state-of-the-art strained techniques being implemented in 90- and 65-nm process technologies. Finally, we conclude with a discussion of the future scalability of strained Si MOSFETs in the ballistic regime and nanoscale CMOS.

PHYSICS OF STRAINED Si

Strained Si has been studied for 50 years, but only recently have some of the subtleties of carrier transport in a strained two-dimensional (2-D) MOSFET inversion layer been fully understood or appreciated [5]–[8]. The carrier mobility is given by

$$\mu = \frac{q\tau}{m^*}, \tag{1}$$

where $1/\tau$ is the scattering rate and m^* is the conductivity effective mass. Strain enhances the mobility by reducing the conductivity effective mass and/or the scattering rate. For electrons, both mass and scattering changes are generally accepted as important for mobility enhancement [9]. However, for holes, only mass change due to band warping and repopulation [7] plays a significant role at today's manufacturable (<1 GPa) stress level since strain-induced valence band splitting is smaller than that for the conduction band. Furthermore, though there has been much focus on reduced in-plane mass to increase mobility, increasing the out-of-plane mass for electrons and holes is now understood to be equally important for maintaining the

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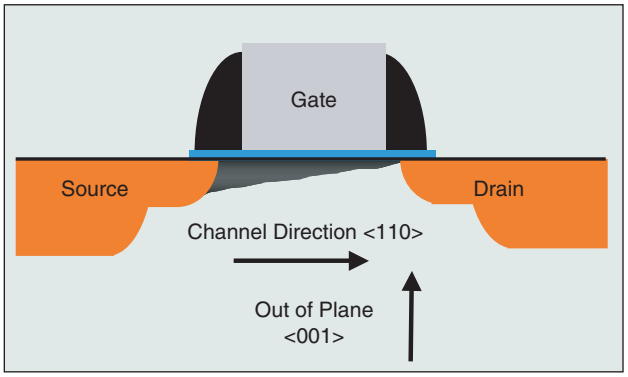


1. MOSFET schematic device cross section (standard orientation).

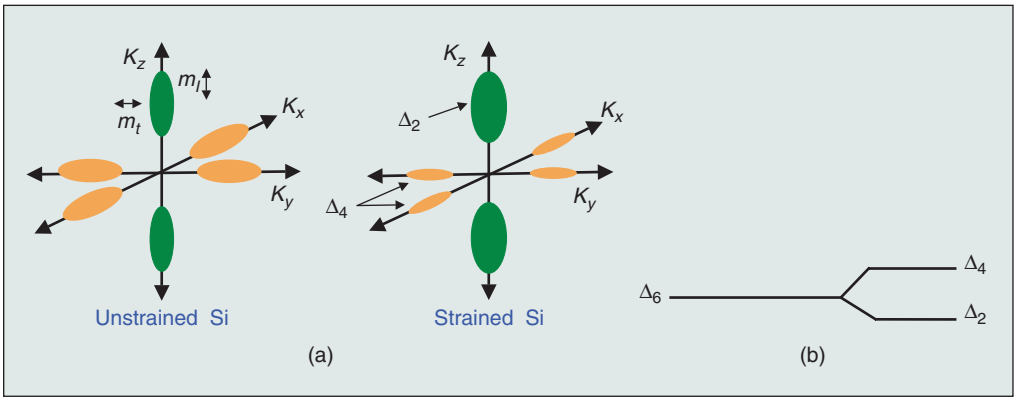
mobility enhancement at high vertical fields (see Figure 1 for definition of in- and out-of-plane).

We first explain electron transport in strained Si. Then we cover hole transport, which, until recently [7], was less well understood but has some interesting physics with practical implications. For electron transport in bulk Si at room temperature, the conduction band is comprised of six degenerate valleys, as shown in Figure 2(a). These valleys are of equal energy, as shown by Δ_6 in Figure 2(b). The degeneracy reflects the cubic symmetry of the Si lattice. The effective mass for any direction is the reciprocal of the curvature of the electron energy function in that direction. Consequently, the effective mass of each ellipsoid is anisotropic, with the transverse mass (perpendicular to the axis) given by $m_t = 0.19\, m_o$ being significantly smaller than the longitudinal mass (parallel to the axis) given by $m_l = 0.98\, m_o$, where m_o is the free electron mass. For unstressed bulk Si, the total electron conductivity mass, m^*, is obtained by adding the contributions of the six degenerate valleys and is given by

$$m^* = \left[\frac{1}{6}\left(\frac{2}{m_l}\right) + \left(\frac{4}{m_t}\right)\right]^{-1}. \qquad (2)$$

For MOSFETs on a (001) wafer, advantageous strain removes the degeneracy between the four in-plane valleys (Δ_4) and the two out-of-plane valleys (Δ_2) by splitting them in energy, as shown in Figure 2(b). The lower energy of the Δ_2 valleys means that they are preferentially occupied by electrons. The electron mobility partly improves via a reduced in-plane and increased out-of-plane m^* due to the favorable mass of the Δ_2 valleys, which results in more electrons with an in-plane transverse effective mass ($m_t = 0.19\, m_o$) and out-of-plane longitudinal mass ($m_l = 0.98\, m_o$). For a given strain, quantifying the effective mass reduction and comparing it to the enhanced mobility reveals that mass reduction alone explains only part of the mobility enhancement [10]. Hence, electron scattering must also be reduced due to the conduction valleys splitting into two sets of energy levels, which lowers the rate of intervalley phonon scattering between the Δ_2 and Δ_4 valleys. Quantifying the improvement due to scattering has been difficult using acceptable scattering parameters, but reduced scattering is still believed to account for the rest of the mobility enhancement [9]. Many types of stress increase the electron mobility via increased population in the Δ_2 valley; in-plane biaxial and uniaxial tensile and out-of-plane uniaxial compressive stress are some examples.

For holes, the valence-band structure of Si is more complex than the conduction-band. It is this complex band structure as well as valence-band warping under strain that results in a much larger hole than electron mobility enhancement. These two factors are also the reason strained p-MOSFETs are a key focus in advanced logic technologies. The band warping is also responsible for the fact that different types of strain (namely, the technologically important biaxial tensile and uniaxial compressive stress) behave differently. For unstrained Si at room temperature, holes occupy the top two bands: the heavy and light hole bands. The unstrained constant energy surfaces for the two bands are shown in Figure 3(a), and they highlight the large heavy hole mass along the $<110>$ direction (common MOSFET channel orientation). With the application of strain, the hole effective mass becomes highly anisotropic due to band warping, and the energy levels become mixtures of the pure heavy, light, and split-off bands. Thus, the light and heavy hole bands lose their meaning, and holes increasingly occupy the top band at higher strain due to the energy splitting. The warped top two bands are shown in Figure 3(b), (c), and (d) for the three most common types of stresses studied by the industry (biaxial tensile and longitudinal uniaxial compressive stress on (100) [6], [11] and (110) wafers [12]). Important to achieving high hole mobility is a low in-plane conductivity mass for

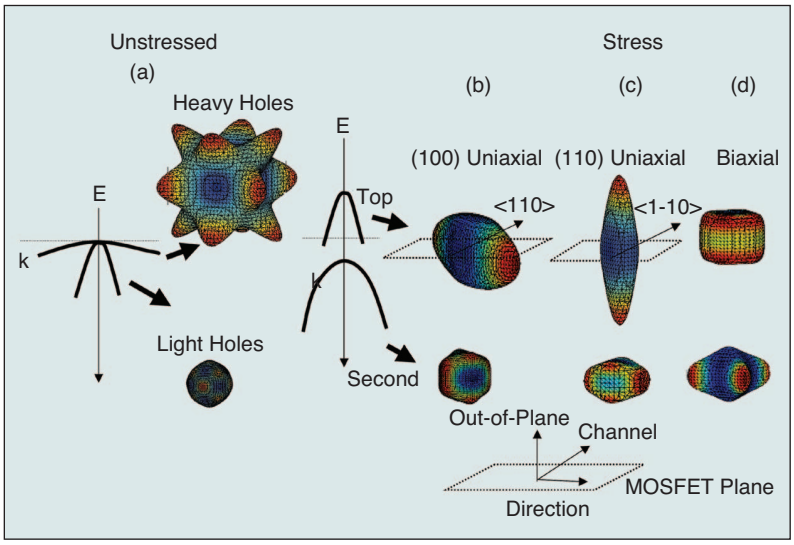


2. (a) Ellipsoids of constant electron energy in reciprocal ("k") space, each corresponding to one of the degenerate conduction band valleys. For this case, the four orange-colored valleys are in the plane of the Si and the two green-colored valleys are out of the plane. (b) Energy level at the bottom of the six conduction band valleys. Application of advantageous strain splits the energy level as shown, removing the degeneracy (i.e., the equivalence in energy) between the Δ_2 and Δ_4 valleys.

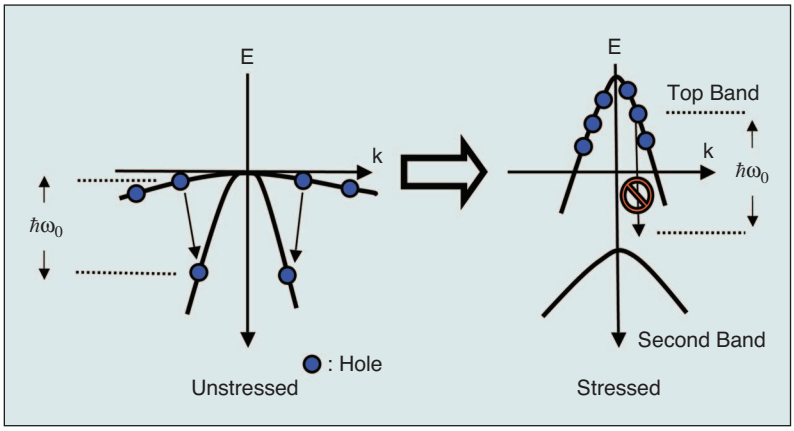
the top band (i.e., a narrow width to the constant energy surface along the channel direction $<110>$). This is due to the difficulty, at manufacturable stress levels, of significantly enhancing hole mobility through reduced intervalley scattering. Hole intervalley scattering is not significantly reduced for stress less than 1 GPa since the band splitting is less than the optical phonon energy (60 meV). Splitting greater than 60 meV and stress greater than 1 GPa are necessary to appreciably suppress intervalley phonon scattering (see Figure 4).

In addition to a low in-plane mass, a high density-of-states in the top band and enough band splitting to populate the top band are also required. As seen in Figure 3(b) and (c), the narrow constant energy surface in the channel direction for uniaxial compression on both (100) and (110) wafers creates a very desirable mass (40% smaller in-plane mass as compared to biaxial tensile stress). Both types of uniaxial stress create a high density-of-states, but only longitudinal uniaxial compressive stress on a (100) wafer creates a large 2-D density-of-states in the plane of the MOSFET (due to the larger mass along $<1,-1,0>$). This helps to maintain a high hole concentration in the top band for compressive stress on a (100) wafer. The increased density-of-states has some effect on the acoustic phonon scattering rate, which is proportional to $m_{\mathrm{DOS}}{}^{3/2}$, but a much smaller effect compared to the in-plane conductivity mass change due to band warping and repopulation. The relative importance of changes in the hole scattering rates for stress less than 1 GPa is debatable, but since biaxial wafer bending [7] and biaxial wafer base stress show negligible mobility enhancement in this range, and mass change is known to be small from band calculations, one can conclude that the scattering changes are small.

Lastly, as seen in Figure 3(d), for biaxial tensile stress, the out-of-plane mass ($z/<001>$ direction [13]) for the second band is larger than that for the top band (the opposite is true for uniaxial compressive stress). Biaxial stress creates a smaller out-of-plane than in-plane top band mass. Figure 5 summarizes the key features for the top band in the simple 2-D energy versus k diagram. This light, top band, out-of-plane mass for biaxial tensile stress creates an interesting effect for carrier transport in the 2-D MOSFET inversion layer. It also explains why, for biaxial tensile stress, the mobility enhancement is lost at high vertical fields, which is not so for the uniaxial stress discussed in this article.



3. Hole constant energy surfaces at 25meV obtained from six band kp calculations for common types of stresses: (a) unstressed, (b) longitudinal compression on (100) wafer, (c) longitudinal compression on (110) wafer, and (d) biaxial tension.

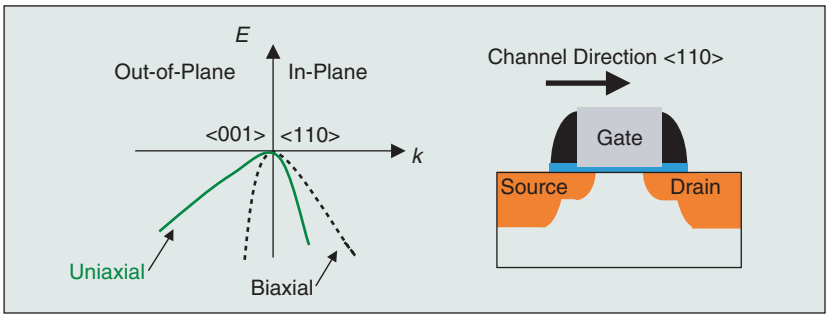


4. Simplified schematic of the hole intervalley phonon scattering process. High stress and splitting larger than the optical phonon energy (60 meV) are required to suppress scattering.

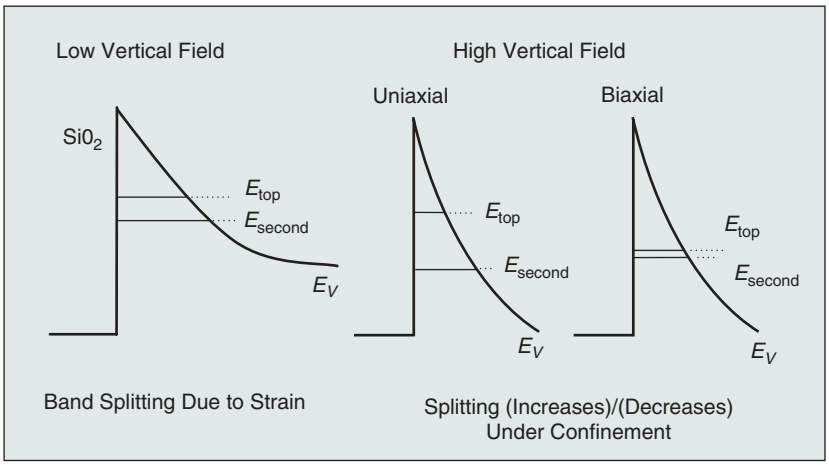
IMPORTANCE OF A LARGER OUT-OF-PLANE MASS FOR THE TOP VERSUS THE SECOND BAND

In a MOSFET, 2-D surface confinement in the inversion layer also shifts the valence bands and the conduction valleys. Whether the confinement-induced shift increases or reduces (cancels) the strain-induced splitting simply depends on the magnitude of the out-of-plane masses (valence band splitting is more complicated, but this simple model captures the essential physics). Bands or valleys with a "light" out-of-plane mass will shift more in energy relative to bands with a "heavy" mass (similar to the increasing ground-state energy of a quantum well as the particle mass decreases). Hence, when the top-most occupied band (or valley) has a lower out-of-plane mass compared to the next occupied band, the splitting is reduced or lost with surface confinement. Figure 6 shows the energy-level shift with confinement for both uniaxial and biaxial stress. E_{top} represents the top band with large out-of-plane mass for uniaxial stress and small out-of-plane mass for biaxial stress (relative to the second band). Hence, the top band will have a small shift in energy due to confinement for uniaxial stress, but a large shift for biaxial stress. E_{second} represents the second band. As seen in the figure, the stress-induced band splitting ($E_{\mathrm{top}} - E_{\mathrm{bottom}}$) increases for uniaxial stress

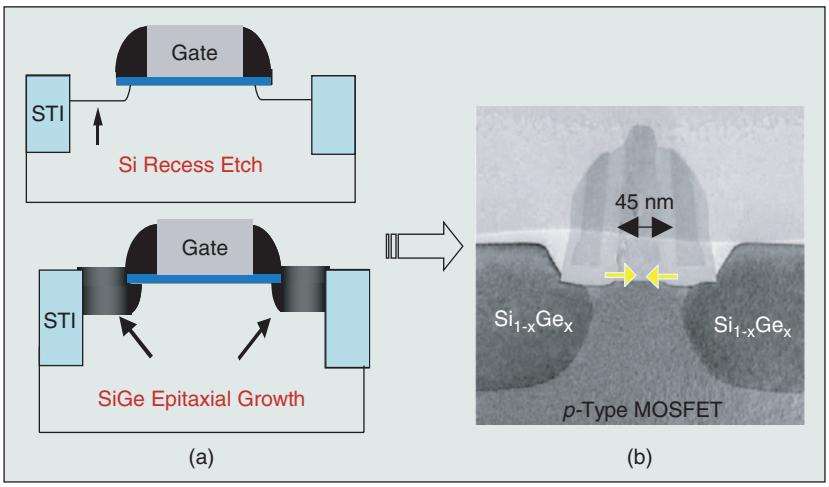
but decreases for biaxial tensile stress. Thus, strain favors occupation of the top band for both types of stresses. Confinement, however, favors occupation of the top band for uniaxial compressive stress and the second band for biaxial tensile stress. The net effect is strain and confinement are additive for uniaxial compressive stress but subtractive for biaxial tensile stress. The competing effects of strain and surface confinement on the band splitting are a factor in the loss in mobility enhancement in biaxially strained Si p-MOSFETs at high electric fields. For uniaxial stress, this increased valence band splitting with confinement maintains the stress-enhanced mobility at high vertical fields; it is one of the key reasons uniaxial stress is being widely adopted [4], [14], [15]. For completeness, in n-MOSFETs at high electric fields, the out-of-plane mass for the Δ_2 valleys is high because, in the out-of-plane direction, the mass is given by the longitudinal mass ($m_l = 0.98\, m_o$). Hence, the band splitting for NMOS at high electric fields is preserved.



5. Simplified valence band energy versus k diagram for strained Si under longitudinal uniaxial compression and biaxial tension.



6. Simplified schematic of valence band splitting of strained Si as a function of gate overdrive.

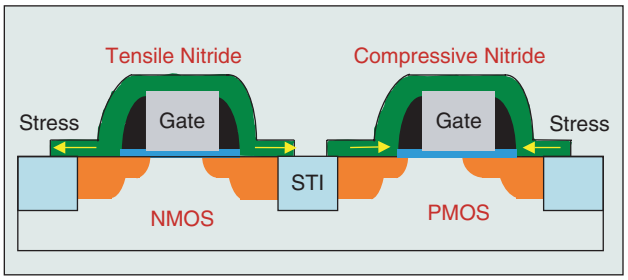


7. (a) Strained Si p-channel MOSFET process flow. (b) TEM cross-sectional view.

STATE-OF-THE-ART STRAIN TECHNOLOGIES

Two basic approaches exist for implementing strain on MOSFETS: a global approach, where stress is introduced across the entire substrate, and a local approach, where stress is engineered into the device by means of epitaxial layers and/or high-stress nitride capping layers. Most of the pioneering work on strained Si has focused on biaxial global stress using a wafer-based approach of a thin strained Si layer on a thick relaxed SiGe virtual substrate. However, for first- and second-generation strained Si MOSFETs [4], [14], [15], the industry is adopting process-induced uniaxial stress. Uniaxial process-induced stress (as opposed to biaxial) is being pursued because larger hole mobility enhancement can be achieved at low strain and because it results in significantly smaller stress-induced n-channel MOSFET threshold voltage shift [7]. Due to these and other differences between uniaxial and biaxial stress, the highest drive current enhancement on short channel devices for uniaxial stress (1.46 mA/μm and 0.88 mA/μm for n- and p-channel devices, respectively) [2] has already significantly surpassed biaxial stress (0.85 mA/μm and 0.45 mA/μm for n- and for p-channel, respectively) [16]. We will next describe three state-of-the-art techniques for introducing uniaxial stress in the Si channel.

In the first approach [4], reported by Intel, Texas Instruments, and Applied Materials Inc. (and recently by IBM [12], TSMC, and Freescale [11]), a local epitaxial film is grown in the source and drain regions and introduces uniaxial stress into the Si channel. The process flow consists of the following steps, as shown in Figure 7(a): the Si source and drain are etched, creating an Si recess, and then SiGe (for p-channel) or SiC (for n-channel) is epitaxially grown in the source and drain. This creates primarily a uniaxial compressive or tensile stress, respectively, in the channel of the MOSFET. For



8. Dual-stress liner process architecture with tensile and compressive Si nitride capping layers over NMOS and PMOS, respectively.

17% Ge, 500–900 MPa of channel stress is created, depending on the proximity of the SiGe to the channel. Impressive 60–90% drive current enhancements on short devices (~35 nm) have been demonstrated, which offers greater device performance than alternative Si device enhancement concepts, such as multigates or high-K dielectrics.

A second, less complex technique for introducing strain in the MOSFET is the use of a tensile and/or compressive capping layer [17], [18], as shown in Figure 8. The capping films are introduced either as a permanent layer post salicide, as discussed here, or as a sacrificial layer before source and drain anneal, as will be discussed next. A dual capping layer approach has been recently enabled by the creation of very high-compressive and high-tensile stress SiN [19]. SiN layers with more than 2 GPa of tensile stress and more than 2.5 GPa of compressive stress have recently been developed by Applied Materials. IBM, AMD, and Fujitsu [17], [18] have reported a CMOS architecture (see Figure 8) in which high-tensile and high-compressive Si nitride layers are selectively deposited on *n*-MOSFET and *p*-MOSFET, respectively. This dual-stress liner (DSL) architecture creates longitudinal uniaxial tensile and compressive stress in the Si channel to simultaneously improve both *n*- and *p*-channel transistors. The process flow consists of a uniform deposition of a highly tensile Si_3N_4 liner post silicidation over the entire wafer, followed by patterning and etching the film off *p*-channel transistors. Next, a highly compressive SiN layer is deposited, and this film is patterned and etched from *n*-channel regions. High-stress compressive films can induce channel stress comparable in magnitude to the first-generation embedded SiGe in the source and drain. The advantages of dual-stress liner flow over epitaxial SiGe are reduced process complexity and integration issues.

Capping layers can also introduce strain into the Si channel via a stress memorization of the poly-Si gate [20]. In this approach, a highly tensile nitride capping layer acts as a temporary stressor. The flow consists of the following steps:

1) poly-Si gate amorphization
2) deposition of a high-stress SiN layer on top of the poly-Si gate
3) recrystallization of the poly-Si gate during source/drain anneal
4) removal of the SiN layer.

After removal of the poly-Si capping layer, some stress remains in the poly-Si gate and Si channel. *n*-channel transistor enhancement of >10 % has been reported with this technique.

FUTURE SCALABILITY OF STRAIN

When pursuing performance features to extend Moore's law, it is important to consider how the performance enhancement scales as the device feature size is reduced. Only device enhancements that are scalable for two to three generations will be adopted by the industry. To investigate the scalability of strain, we start with the classical MOSFET equations for long-channel devices that show that drain current is proportional to the mobility.

$$I_{d(\mathrm{lin})} = \frac{\mu W C_{\mathrm{ox}}}{L}\left(V_g - V_t - \frac{V_d}{2}\right)V_d \tag{3}$$

$$I_{d(\mathrm{sat})} = \frac{\mu W C_{\mathrm{ox}}}{2L}\left(V_g - V_t\right)^2. \tag{4}$$

However, as the MOSFET carrier transport becomes ballistic, the carrier transport can best be described by carrier injection at the source [21]. The drain current in saturation, I_d, is given by

$$I_{d(\mathrm{sat})} = WC_{\mathrm{ox}} < \upsilon(0) > (V_g - V_t), \tag{5}$$

where $\langle \upsilon(0) \rangle$ is the average velocity of carriers at the source and $C_{\mathrm{ox}}(V_{gs} - V_t)$ is the charge density [21]. In the limit where channel length goes to zero, $\langle \upsilon(0) \rangle$ is the unidirectional thermal velocity υ_T, since the velocity at the beginning of the channel is set by carriers injected from the thermal equilibrium source [22]. υ_T is given by

$$\upsilon_T = \sqrt{\frac{2k_B T_{\mathrm{L}}}{\pi m_t^*}}, \tag{6}$$

and T_{L} is the lattice temperature. Thus, in the nanoscale channel limit, the drain current becomes

$$I_d = WC_{\mathrm{ox}}\sqrt{\frac{2k_B T_{\mathrm{L}}}{\pi m_t^*}}(V_g - V_t). \tag{7}$$

From (7), it can be seen that strain-induced reductions in the effective mass will still enhance the drive current in ballistic MOSFETs, which has been a historical concern for mobility-enhancement techniques.

Furthermore, at strain levels higher than those in state-of-the-art production today, the effective mass continues to decline due to increased repopulation of valleys/bands (more so for holes). Also, at higher strain, the valence band splitting (~25 meV at 100 MPa to ~55 meV at 1 GPa) becomes greater than the optical phonon energy, which will further enhance the mobility by a reduction in the scattering rate. Experimental and theoretical work suggests much larger mobility enhancement is achievable at higher strain. Ratios of stressed to unstressed mobilities of 4 and 1.7 have been reported experimentally for holes and electrons, respectively [23]. The problem of dislocations in the strained layer at higher levels of strain will have to be addressed by changing thermal cycles and controlling growth.

CONCLUSION

Strain introduces advantageous anisotropy in Si by altering its valence and conduction band structures, which reduces the effective mass and/or scattering rates. Strain is being adopted in all high-performance logic technologies. SiGe in the source and drain, dual stress liners, and stress memorization techniques have all been introduced in state-of-the-art MOSFETS. Strain will continue to scale well into future logic technology generations as the MOSFET enters the ballistic regime.

REFERENCES

[1] V. Chan, R. Rengarajan, N. Rovedo, W. Jin, T. Hook, P. Nguyen, J. Chen, E. Nowak, X. Chen, D. Lea, A. Chakravarti, V. Ku, S. Yang, A. Steegen, C. Baiocco, P. Shafer, H. Ng, S. Huang, and C. Wann, "High speed 45 nm gate length MOSFETs integrated into a 90 nm bulk technology incorporating strain engineering," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2003, pp. 77–80.

[2] P. Bai C. Auth, S. Balakrishnan, M. Bost, R. Brain, V. Chikarmane, R. Heussner, M. Hussein, J. Hwang, D. Ingerly, R. James, J. Jeong, C. Kenyon, E. Lee, S.H. Lee, N. Lindert, M. Liu, Z. Ma, T. Marieb, A. Murthy, R. Nagisetty, S. Natarajan, J. Neirynck, A. Ott, C. Parker, J. Sebastian, R. Shaheed, S. Sivakumar, J. Steigerwald, S. Tyagi, C. Weber, B. Woolery, A. Yeoh, K. Zhang, and M. Bohr, "A 65 nm logic technology featuring 35 nm gate lengths, enhanced channel strain, 8 Cu interconnects layers, low-k ILD and 0.57 um2 SRAM cell," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2004, pp. 657–660.

[3] P.R. Chidambaram, B.A. Smith, L.H Hall, H. Bu, S. Chakravarthi, Y. Kim, A.V. Samoilov, A.T. Kim, P.J. Jones, R.B. Irwin, M.J Kim, A.L.P Rotondaro, C.F Machala, and D.T. Grider, "35% drive current improvement from recessed-SiGe drain extensions on 37 nm gate length PMOS," in *Proc. Symp. VLSI Technology*, 2004, pp. 48–49.

[4] S.E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Ma Zhiyong, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology featuring strained silicon," *IEEE Electron Device Lett.,* vol. 25, pp. 191–193, Apr. 2004.

[5] J. Welser, J.L. Hoyt, and J.F. Gibbons, "Electron mobility enhancement in strained-Si N-Type metal-oxide-semiconductor field-effect transistors," *IEEE Electron Device Lett.,* vol. 15, pp. 100–102, Mar. 1994.

[6] D.K. Nayak and S.K. Chun, "Low-field hole mobility of strained Si on (100) Si1-xGex substrate," *Appl. Phys. Lett.,* vol. 64, pp. 2514–2516, Jan. 1994.

[7] S.E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs," in *Tech. Digest IEEE Int. Electron Devices Meeting*, 2004, pp. 221–224.

[8] M.V. Fischetti and S.E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys*., vol. 80, no. 4, pp. 2234–2252, Aug. 1996.

[9] C. Zhi-Yuan, M.T. Currie, C.W. Leitz, G. Taraschi, E.A. Fitzgerald, J.L. Hoyt, and D.A. Antoniadis, "Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates," *IEEE Electron Device Lett.,* vol. 22, pp. 321–323, July 2001.

[10] S.-i. Takagi, J.L. Hoyt, J. Welser, and J.F. Gibbons, "Comparative study, of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 80, no. 3, pp. 1567–1577, Aug. 1996.

[11] D. Zhang, B.Y. Nguyen, T. White, B. Goolsby, T. Nguyen, V. Dhandapani, J. Hildreth, M. Foisy, V. Adams, Y. Shiho, A. Thean, D. Theodore, M. Canonico, S. Zollner, S. Bagchi, S. Murphy, R. Rai, J. Jiang, M. Jahanbani, R. Noble, M. Zavala, R. Cotton, D. Eades, S. Parsons, P. Montgomery, A. Martinez, B. Winstead, M. Mendicino, J. Cheek, J. Liu, P. Grudowski, N. Ranami, P. Tomasini, C. Arena, C. Werkhoven, H. Kirby, C.H. Chang, C.T. Lin, H. C. Tuan, Y. C. See, S. Venkatesan, V. Kolagunta, N. Cave, and J. Mogab, "Embedded SiGe S/D PMOS on thin body SOI substrate with drive current enhancement," in *Symp. VLSI Technology,* 2005, pp. 26–27.

[12] Q. Ouyang, M. Yang, J. Holt, S. Panda, H. Chen, H. Utomo, M. Fischetti, N. Rovedo, J. Li, N. Klymko, H. Wildman, T. Kanarsky, G. Costrini, D.M. Fried, A. Bryant, J.A. Ott, M. Ieong, and C.-Y. Sung, "Investigation of CMOS devices with embedded SiGe source/drain on hybrid orientation substrates," in *Symp. VLSI Technology,* 2005, pp. 28–29.

[13] C.Y.-P Chao and S.L. Chuang, "Spin-orbit-coupling effects on the valence-band structure of strained semiconductor quantum wells," *Phys. Rev.,* vol. B 46, no. 7, pp. 4110–4122, Aug. 1992.

[14] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2003, pp. 11.6.1–11.6.3.

[15] M.D. Giles, M. Armstrong, C. Auth, S.M. Cea, T. Ghani, T. Hoffmann, R. Kotlyar, P. Matagne, K. Mistry, R. Nagisetty, B. Obradovic, R. Shaheed, L. Shifren, M. Stettler, S. Tyagi, X. Wang, C. Weber, and K. Zawadzki, "Understanding stress enhanced performance in Intel 90 nm technology," in *Proc. Symp. VLSI Technology*, 2004, p. 118.

[16] H.C.H-Wang, Y.-P. Wang, S.-J. Chen, C.-H. Ge, S.M. Ting, J.-Y. Kung, R.-L. Hwang, H.-K. Chiu, L.C. Sheu, P.-Y. Tsai, L.-G. Yao, S.-C. Chen, H.-J. Tao, Y.-C. Yeo, W.-C. Lee, and C. Hu, "Substrate-strained silicon technology: Process integration," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2003, pp. 3.4.1–3.4.4.

[17] S. Pidin, T. Mori, K. Inoue, S. Fukuta, N. Itoh, E. Mutoh, K. Ohkoshi, R. Nakamura, K. Kobayashi, K. Kawamura, T. Saiki, S. Fukuyama, S. Satoh, M. Kase, and K. Hashimoto, "A novel strain enhanced CMOS architecture using selectively deposited high tensile and high compressive silicon nitride films," Fujitsu, Ltd., Tokyo, Japan, IEDM 2004.

[18] H. S Yang, R. Malik, S. Narasimha, Y. Li, R. Divakaruni, P. Agnello, S. Allen, A. Antreasyan, J. C. Arnold, K. Bandy, M. Belyansky, A. Bonnoit, G. Bronner, V. Chan, X. Chen, Z. Chen, D. Chidambarrao, A. Chou, W. Clark, S. W. Crowder, B. Engel, H. Harifuchi, S. F. Huang, R. Jagannathan, F. F. Jamin, Y. Kohyama, H. Kuroda, C.W. Lai, H.K. Lee, W.-H Lee, E.H Lim, W. Lai, A. Mallikarjunan, K. Matsumoto, A. McKnight, J. Nayak, H.Y. Ng, S. Panda, R. Rengarajan, M. Steigerwalt, S. Subbanna, K. Subramanian, J. Sudijono, G. Sudo, S.-P. Sun, B. Tessier, Y. Toyoshima, P. Tran, R. Wise, R. Wong, I.Y. Yang, C.H. Wann, L.T. Su, M. Horstmann, Th. Feudel, A. Wei, K. Frohberg, G. Burbach, M. Gerhardt, M. Lenski, R. Stephan, K. Wieczorek, M. Schaller, H. Salz, J. Hohage, H. Ruelke, J. Klais, P. Huebler, S. Luning, R. van Bentum, G. Grasshoff, C. Schwan, E. Ehrichs, S. Goad, J. Buller, S. Krishnan, D. Greenlaw, M. Raab, and N .Kepler, "Dual stress liner for high performance sub-45 nm gate length SOI CMOS manufacturing," in *Tech. Dig. IEEE Int. Electron Devices Meeting*, 2004, pp. 1075–1077.

[19] A. A-. Bayati, L. Washington, L.-Q Xia, M. Balseanu, Z. Yuan, M. Kawaguchi, F. Nouri, and R. Arghavani, "Production processes for inducing strain in CMOS channels," *Semiconductor Fabtech*, 26th ed., 2005, pp. 84–88.

[20] C.Chien-Hao, T.L. Lee, T.H Hou, C.L. Chen, C.C. Chen, J.W. Hsu, K.L. Cheng, Y.H Chiu, H.J. Tao, Y. Jin, C.H. Diaz, S.C. Chen, and M.-S. Liang, "Stress memorization technique (SMT) by selectively strained-nitride capping for sub-65 nm high-performance strained-Si device application," in *Proc. Symp. VLSI Technology,* 2004, pp. 56–57.

[21] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *IEEE Trans. Electron Devices,* vol. 49, pp. 133–141, Jan. 2002.

[22] M. Lundstrom, "Device physics at the scaling limit: What matters? [MOSFETs]," in *Proc. IEEE Int. Electron Devices Meeting,* 2003, pp. 1-4.

[23] J.L Hoyt, H.M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E.A. Fitzgerald, and D.A. Antoniadis, "Strained silicon MOSFET technology," in *Tech. Digest IEEE Int. Electron Devices Meeting*, Washington, 2002, pp. 23–26.

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