



PIONEERS IN
COLLABORATIVE
RESEARCH®



ITRS PIDS Meeting

San Francisco Marriott
July 14–16, 2008

Kwok Ng
PIDS U.S. Chair
SRC

- PIDS Roster
- Surveys of Physical Gate Lengths
 - Logic
 - DRAM
- Adopting New Physical Gate Length L_g Scaling
- 2008 Update: Schedule & Responsibility
- Other Areas: NVM, DRAM, Reliability?
- Speed Metric: $CV//I$
- R_{sd} Specs
- Summary (public presentation)

Name	Group	Name	Group	Name	Group	Name	Group
US		Japan				Europe	
Ng, Kwok (US Chair & ITWG rep)	Logic (Lead)	Oda, Hidekazu (Japan Chair)	Logic	Ogura, Mototsugu	Logic	Skotnicki, Thomas (Europe Chair)	Logic (Lead)
Brewer, Joe E.	NVM	Inoue, Hirofumi (Japan V-Chair)	NVM	Sawada, Shizuo	DRAM (lead)	DeMeyer, Kristin	Logic
Chang, Chorng-Ping?	?	Akasaka, Yasushi	Logic	Shibahara, Kentaro	Logic	Jurczak, Malgorzata	
Dellin, Theodore A. (Ted)	Reliab (Lead)	Eimori, Takahisa	Logic	Sugii, Toshihiro	Logic	Lander, Robert	Logic
Duane, Michael		Hiramoto, Toshiro	Logic	Tadaki, Yoshitaka	DRAM	Poiroux, Thierry	Logic
Hutchby, Jim?	ERD/ERM ?	Hori, Atsushi	NVM	Tagawa, Yukio	Logic	Schruefer, Klaus	Logic
Maszara, Witek	Logic	Ida, Jiro	Logic	Takagi, Shinnichi	Logic	Taiwan	
Ning, Tak H.	Logic	Imai, Kiyotaka	Logic	Tanaka, Tetsu	Logic	Liu, Rich (Taiwan Co-Chair)	NVM (Lead)
Prall, Kirk	DRAM/NVM	Kasai, Naoki	NVM	Yoshimi, Makoto	Logic	Ma, Mike (Taiwan Co-Chair)	Logic
Tsai, Wilman	Logic	Mifuji, Michihiko	Logic			Diaz, Carlos	Logic
Wu, Jeff	Logic					See, Yee-Chaung	Logic
Yeap, Geoffrey	Logic						
Yu, Scott	Logic						
Zeitsoff, Peter M.	Logic						

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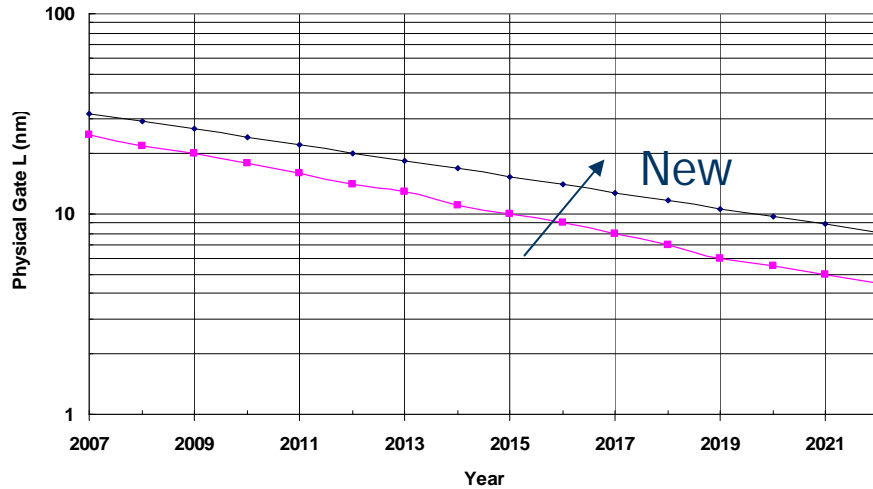
- PIDS Roster
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- **Adopting New Physical Gate Length L_g Scaling**
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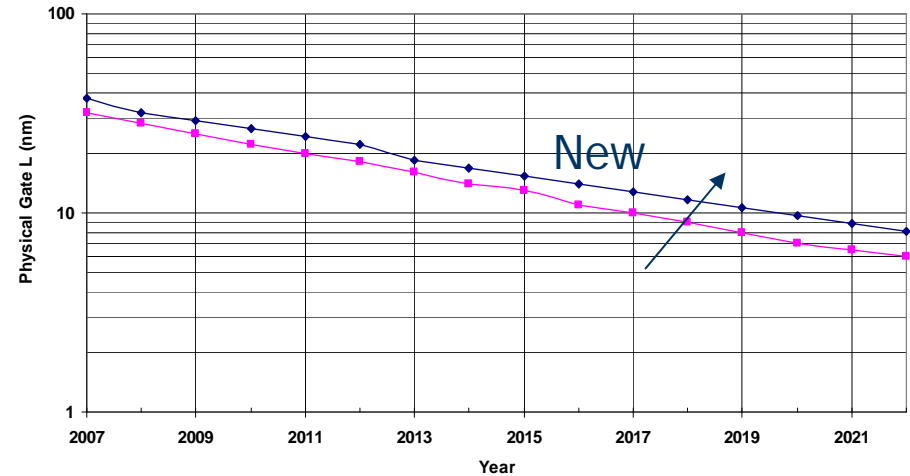
New vs. Current Physical Gate Length Projections



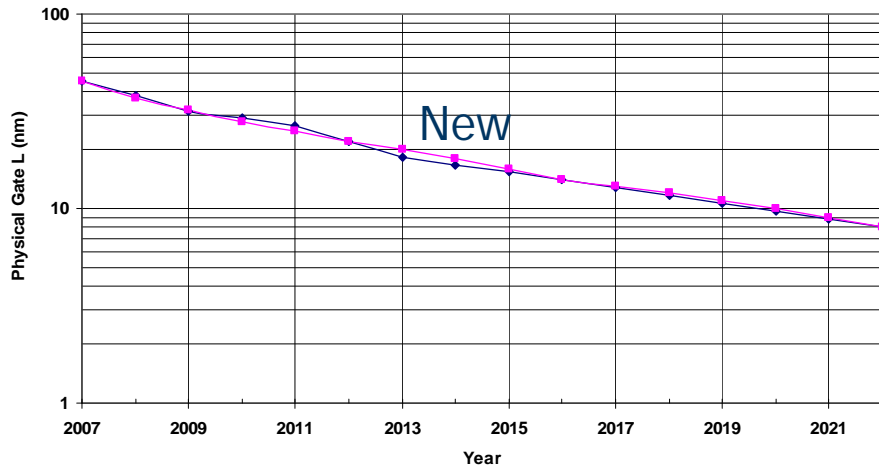
MPU Shift



LOP Shift



LSTP Shift



- MPU physical gate L shifts by 3-5 yrs
- LOP physical gate L shifts by 1-3 yrs
- LSTP physical gate L minor shift

- Speed scaling also slowed down from 15%/yr to 8%/yr.

- Adopt common slowed-down scaling model proposed by IRC, for 2008 tables and beyond.
- Major changes: HP logic and LOP physical gate lengths.
Both shift and change of slope.
- Original Plan for PIDS 2008 Update (following FEP strategy)
 - Shift relevant rows by constant 3 (or 2) years. Keep others same. Slope remains unchanged.
 - Use 2005 Table for years 2008/2009. Leave 2007 blank.
 - In major year 2009, adopt the IRC numbers fully (shift and change slope), and do new calculations accordingly.
- Alternative Plan
 - Adopt IRC rules fully instead of simple shift.
 - Shift and “interpolate” data. No real calculation.

2007 Table

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
MPU/ASIC Phys Lg (nm)	25	22	20	18	16	14	13	11	10
EOT (A)	11	9	7.5	6.5	5.5	5			

2008 Table (shift by 3 year.
Incorporate ORTC rules in 2009)

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
MPU/ASIC Phys Lg (nm)				25	22	20	18	16	14
EOT (A)				11	9	7.5	6.5	5.5	5

2008 Table (adopt ORTC rules right away
and do “interpolation” [no real calculation])

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
ORTC MPU Lg (nm)	32	29	27	24	22	20	18	17	15
EOT (A)					9	7.5	6.5	6.0	5.25

shift

interpolate

Sample Using New IRC L_g Scaling Rule

2008

Table PIDS2

High-performance Logic Technology Requirements—Near and Long-term Years

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
L_g : Physical Gate for High Performance logic (nm) [1]	32	29	27	24	22	20	18	17	15	14	12.8	11.7	10.7	9.7	8.9	8.1
EOT: Equivalent Oxide Thickness [2]																
Extended planar bulk (Å)		11.3	11	10.3	9	7.5	6.5	6	5.25	5						
UTB FD (Å)							7	6.5	6.75	5.5	5	5	5			
DG (Å)									7.5	7	6	6	6	5.8	5.5	5.5
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]																
Extended Planar Bulk (Å)		7.4	7.4	6	3.1	2.9	2.8	2.75	2.65	2.6						
UTB FD (Å)							4	4	4	4	4	4	4			
DG (Å)									4	4	4	4	4	4	4	4
EOT _{inv} : Electrical Equivalent Oxide Thickness in inversion [4]																
Extended Planar Bulk (Å)		18.6	18.4	16.3	12.1	10.4	9.3	8.8	7.9	7.6						
UTB FD (Å)							11	10.5	9.8	9.5	9	9	9			
DG (Å)									11.5	11	10	10	10	9.9	9.5	9.5
$J_{g,inv}$: Maximum gate leakage current density [5]																
Extended Planar Bulk (A/cm ²)		449	624	836	909	1000	1110	1180	1340	1430						
UTB FD (A/cm ²)							1110	1180	1340	1430	1568	1722	1874			
DG (A/cm ²)									1340	1430	1568	1722	1874	2066	2220	2500
V_{dd} : Power Supply Voltage (V) [6]																
Extended Planar Bulk (V)		1.1	1.1	1.07	1	1	1	0.975	0.925	0.9						
UTB FD and DG (V)							1	1	0.95	0.9	0.9	0.9	0.9	0.8	0.8	0.7
$V_{t,inv}$: Saturation Threshold Voltage [7]																
Extended Planar Bulk (mV)		175	167	121	94	94	103	102	107	112						
UTB FD (mV)							103	96	88	87	94	97	99			
DG (mV)									110	105	104	106	109	111	110	109
$I_{sub,inv}$: Source/Drain Subthreshold Off-State Leakage Current [8]																
Extended Planar Bulk (μA/μm)		0.13	0.17	0.46	0.71	0.7	0.64	0.69	0.71	0.68						
UTB FD (μA/μm)							0.33	0.43	0.57	0.62	0.56	0.55	0.57			
DG (μA/μm)									0.27	0.34	0.37	0.38	0.38	0.4	0.44	0.48
$I_{d,inv}$: NMOS Drive Current [9]																
Extended Planar Bulk (μA/μm)		1102	1153	1312	1513	1639	1807	1816	1793	1762						
UTB FD (μA/μm)							1948	1970	1970	1944	2123	2197	2181			
DG (μA/μm)									1930	1943	2220	2309	2344	2395	2627	2533
Mobility enhancement factor due to strain [10]				1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8

Too relaxed?

Smaller for metal gate?

Color. Metal gate already here?

Color? Valley?

Color?

Valley?

Peak?

2008														
Table PIDS3c and d Low Operating Power Technology Requirements—Near and Long-term Years														
Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or														
Year in Production	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
L _g : Physical gate length for LOP (nm) [1]	38	32	29	27	24	22	18	17	15	14	12.8	11.7	10.7	9.7
EOT: Equivalent Oxide Thickness [2]														
Extended planar bulk (Å)	13.1	12	11.3	10.7	9.7	9	8							
UTB FD (Å)							9	8.5	8	8	7.9	7.35		
DG (Å)							9	9	8.5	8	8	8	7.7	7
Gate Poly Depletion and Inversion-Layer Equivalent Thickness [3]														
Extended planar bulk (Å)	6.5	6.4	4.2	3.37	3.3	3.4	3.2							
UTB FD (Å)							4	4	4	4	4	4		
DG (Å)							4	4	4	4	4	4	4	4
EOT _{elec} : Electrical Equivalent Oxide Thickness in inversion [4]														
Extended planar bulk (Å)	19.6	18.4	15.4	14	13	12.4	11.2							
UTB FD (Å)							13	12.5	12	12	11.9	11.4		
DG (Å)							13	13	12.5	12	12	12	11.7	11
J _{g,limit} : Maximum gate leakage current density [5]														
Extended Planar Bulk (A/ cm ²)	40	78	86	93	105	114	139							
UTB FD (A/ cm ²)							139	148	168	179	196	215		
DG (A/ cm ²)							139	148	168	179	196	215	234	258
V _{dd} : Power Supply Voltage (V) [6]														
Extended Planar Bulk (V)	0.9	0.8	0.8	0.8	0.77	0.7	0.7							
UTB FD (V)							0.7	0.65	0.6	0.6	0.59	0.54		
DG (V)							0.7	0.65	0.6	0.6	0.6	0.6	0.57	0.5
V _{i,sat} : Saturation Threshold Voltage [7]														
Extended Planar Bulk (mV)	301	294	296	294	279	259	249							
UTB FD (mV)							209	202	199	202	201	193		
DG (mV)							202	203	202	201	202	202	198	190
I _{sd,leak} : Source/Drain Subthreshold Off-State Leakage Current [8]														
Extended Planar Bulk (μA/μm)	3.00E-03	9.08E-03	7.78E-03	7.89E-03	1.21E-02	1.83E-02	3.57E-02							
UTB FD (μA/μm)							1.19E-02	1.61E-02	1.94E-02	1.86E-02	2.15E-02	3.10E-02		
DG (μA/μm)							7.73E-03	8.17E-03	9.66E-03	1.07E-02	1.12E-02	1.24E-02	1.59E-02	2.14E-02

2008														
<i>Table PIDS3c and d Low Operating Power Technology Requirements—Near and Long-term Years</i>														
Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or														
Year in Production	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
L _g : Physical gate length for LOP (nm) [1]	38	32	29	27	24	22	18	17	15	14	12.8	11.7	10.7	9.7
I _{d,sat} : NMOS Drive Current [9]														
Extended Planar Bulk (μA/μm)	605	563	670	723	734	682	760							
UTB FD (μA/μm)							788	768	755	763	801	749		
DG (μA/μm)							821	788	790	826	895	908	884	821
Mobility enhancement factor due to strain [10]		1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8
I _{d,sat} enhancement factor due to strain [11]														
Extended Planar Bulk	1.11	1.15	1.12	1.11	1.11	1.11	1.09							
UTB FD							1.07	1.07	1.07	1.06	1.06	1.06		
DG							1.05	1.05	1.05	1.05	1.04	1.04	1.04	1.04
Effective Ballistic Enhancement Factor [12]														
Extended Planar Bulk	1	1	1	1	1	1	1							
UTB FD							1	1.05	1.1	1.1	1.16	1.21		
DG							1	1.08	1.17	1.18	1.25	1.26	1.29	1.37
R _{sd} : Effective Parasitic series source/drain resistance [13]														
Extended Planar Bulk (Ω-μm)	180	190	190	190	190	190	190							
UTB FD (Ω-μm)							190	185	175	170	165	162		
DG (Ω-μm)							180	180	180	180	170	170	166	154
C _{g,ideal} : Ideal NMOS Device Gate Capacitance [14]														
Extended Planar Bulk (F/μm)	6.68E-16	6.01E-16	6.53E-16	6.63E-16	6.36E-16	6.13E-16	5.54E-16							
UTB FD (F/μm)							4.78E-16	4.69E-16	4.31E-16	4.02E-16	3.68E-16	3.35E-16		
DG (F/μm)							4.78E-16	4.52E-16	4.14E-16	4.02E-16	3.68E-16	3.36E-16	3.15E-16	3.04E-16
C _{g,total} : Total gate capacitance for calculation of CV/I [15]														
Extended Planar Bulk (F/μm)	9.08E-16	8.41E-16	8.93E-16	9.00E-16	8.56E-16	8.13E-16	7.54E-16							
UTB FD (F/μm)							6.88E-16	6.74E-16	6.31E-16	6.02E-16	5.50E-16	5.29E-16		
DG (F/μm)							7.18E-16	6.92E-16	6.54E-16	6.43E-16	6.08E-16	5.76E-16	5.46E-16	5.11E-16

- Need to fix first few years to reflect incorporation of high-K and metal gate.
 - Leave them “as is”?
 - Recalculate first ~3 years?

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- Other Areas: NVM, DRAM, Reliability?
 - Reliability: Need change? Need new member (only 1 now & retiring)?
- Speed Metric: CV/I
- R_{sd} Specs

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ITRS is driven by “speed” performance

Currently using $CV//$

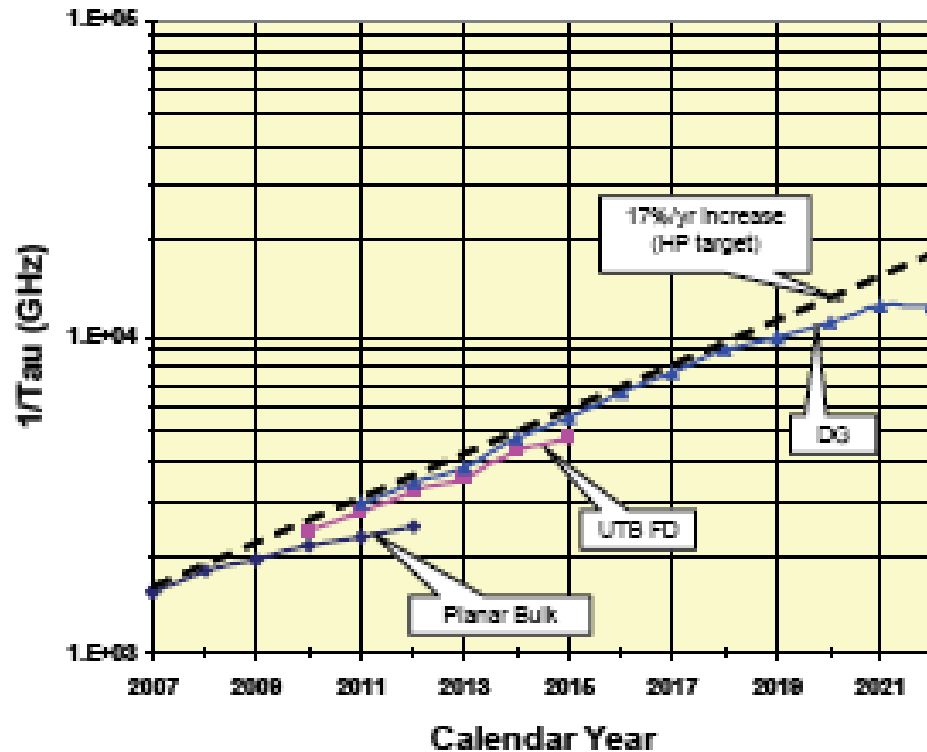


Figure PIDS1 High-Performance Logic: Scaling of Transistor Intrinsic Speed, $1/\tau$

V	C	I	CV/I represents	Max Cir f
$V_{dd} - V_t$	Intrinsic gate (channel)	I_{on}	Transit time (t_t)	$\ll 1/2t_t?$
V_{dd}	Intrinsic gate (channel)	I_{on}	$>$ Transit time (t_t)	$\ll 1/2t_t?$
$V_{dd} - V_t$	Intrinsic gate + gate fringing/parasitics	I_{on}	Cut-off freq (small-sig unity gain) $C/gm = 1/f_t$	$< f_t ?$
V_{dd}	Intrinsic gate + gate fringing/parasitics	I_{on}	τ in ITRS. Rise/fall time	$\ll 1/2\tau ?$
V_{dd}	Both n - & p -chan gates, + drain cap, + runners	I_{eff}	Ring oscillator delay per stage. Ave charge/discharge time = $CV/2I = t_r$	$\sim 1/2t_r$

Note factor of 2 for circuit (charge & discharge)

$$V = V_{dd} - V_T$$

$$\frac{C(V - V_T)}{I} = \frac{C_A WL(V - V_T)}{C_A (V - V_T) v W} = \frac{L}{v} = t_t$$

$$V = V_{dd}$$

$$\frac{CV}{I} = \frac{C_A WL V}{C_A (V - V_T) v W} = \frac{LV}{(V - V_T) v} = \frac{t_t V}{V - V_T}$$

- Transit time t_t :
 - It is the **response time** of the device.
 - It is “device” speed, not “circuit” speed.
 - Does not include parasitics such as C_{drain} .
In SOI or FinFET fails to show advantages of reduced C_{drain} .
- Cut-off frequency f_t (unity current gain):
 - Max circuit frequency $< f_t$?
 - This is small-signal frequency. Large-signal should be slower?
- τ in ITRS:
 - Same argument as above. $1/\tau$ is **not** “circuit” speed.
 - Factor of 2 missing!
- Ring-oscillator delay t_r :
 - **This is the fastest circuit speed realizable!?**
 - If yes, any speed parameter faster is not appropriate!

- CV/I is a good speed metric, but what C , V , I should we use?
- Current C , V , I values:
 - Does not represent circuit speed, although it may track. (Proportional at best. Not for SOI or FinFET.)
 - Does not take into account of p -channel performance.
 - Factor of 2 missing?
- PIDS table does not show C value (intrinsic gate + parasitics). Without it, it is still a black-box to users.
- We can use appropriate values (C , V , I) to get ring-oscillator speed (or close).
- Should we keep on doing same, or change (add) it in major year 2009?

Effect on linear region:

$$R_{ch} = \frac{L_{ch}}{W_{ch} Q \mu} = \frac{15\text{nm}}{1\mu\text{m} \times (V_{dd} - V_t)(3.45 \times 10^{-6}) \times 300}$$

$$= 16 \Omega\text{-}\mu\text{m}$$



Total = $216 \Omega\text{-}\mu\text{m}$

Effect on speed has to be calculated.

Probably OK?

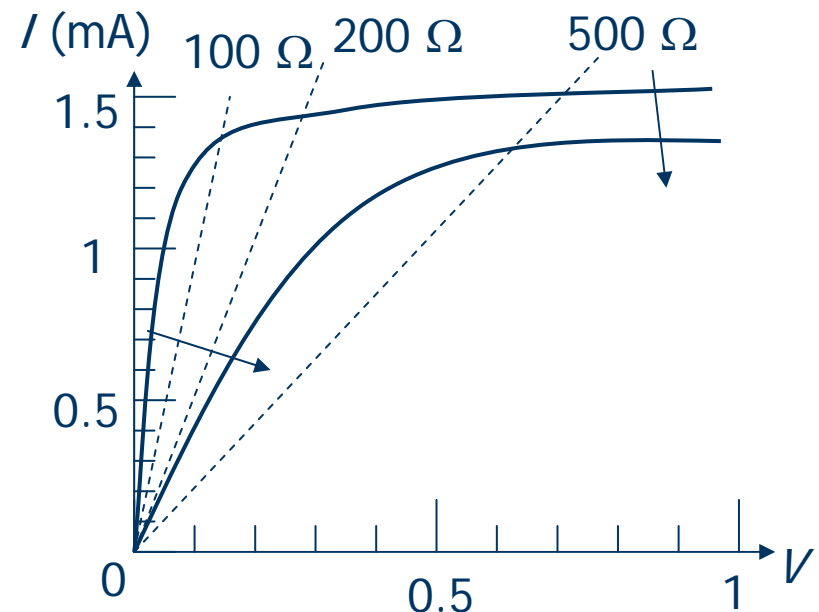
Effect on saturation region:

$$\Delta V_{gs} = IR_s = 100 \times 1.5 \text{mA} = 150 \text{mV}$$

$$\frac{\Delta V_{gs}}{V_{dd} - V_t} = \frac{150}{1000 - 100} = 17\% \quad \text{Gate overdrive reduction}$$

Is this acceptable?

Combined effect probably $> 20\%$



PIDS Summary

July 16, 2008
San Francisco, CA

Kwok Ng

Rich Liu

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SRC/USA

Macronix/Taiwan

Applied Materials/USA

Renesas/Japan

Toshiba/Japan

- Japan PIDS team provided survey on L_g (physical gate lengths) for HP, LSTP, and LOP logic devices, helping to establish new slowed-down scaling model.
- 2008 update will adopt new L_g rules proposed by ORTC.
- Discussion of adding ring-oscillator speed as circuit-speed metric, in addition to current form of CV/I .

- HP and LOP devices using new L_g rules. LSTP devices remain same.
- Some “bumps” in first ~3 years, due to merging of 2005 & 2007 tables.
- To reflect incorporation of high-K dielectrics and metal gate, plan to re-calculate first ~3 years.
- UTB-FD and DG follow delay of L_g rules.
- Reconsider series resistance R_{sd} specs.

- Fix inconsistency in 2007 tables between ORTC & PIDS.
- PIDS table:
 - L_g values using 2nd-best figures among 5 companies in DRAM WG survey.
 - L_g follows 2.5-yr cycle 2007–2009, and 3-yr cycle 2009–2022.
 - Cell size calculated with HP numbers in table.
- ORTC table:
 - L_g follows 3-yr cycle 2007–2022.
 - Cell size calculated with rounded HP number.



Summary on Nonvolatile Memory



- No change in 2008 update, for both NAND flash & NOR flash scaling.
- Now preparing for survey for 2009 ITRS.