A Low-Cost Fully Self-Aligned SiGe BiCMOS Technology Using Selective Epitaxy and a Lateral Quasi-Single-Poly Integration Concept

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***Abstract*—We present a low-cost concept for a self-aligned SiGe heterojunction bipolar transistor (HBT). In conventional double-poly HBTs, the base link is formed by use of a sacrificial layer to grow the SiGe epitaxy between an external base polysilicon and the silicon substrate, resulting in a vertical base link. In this concept, the SiGe epitaxy is laterally connected to the extrinsic base poly forming a short and fully self-aligned base link. While strongly reducing process complexity, this concept maintains a minimal link resistance between the internal and the external base. We demonstrate the integration of this HBT with balanced dc and ac performance in a 0.25-μm bipolar complementary metal–oxide–semiconductor technology, featuring all passive devices necessary for RF design. The bipolar multitransistor yield shows similar values compared to our conventional double-poly integration concept.**

***Index Terms*—Bipolar complementary metal–oxide–semiconductor (BiCMOS), SiGe epitaxy, silicon-germanium (SiGe).**

I. Introduction

TODAY, silicon–germanium (SiGe)-based bipolar complementary metal–oxide–semiconductor (BiCMOS) technology is becoming well established for radio frequency integrated circuits (ICs), applied, e.g., for mobile communications or high-speed data links. Recent advances in SiGe bipolar technology allowed astounding values for the maximum transit frequency $f_{t,\max}$ up to 350 GHz [1]. Also, the integration of SiGe bipolar transistors in highly advanced CMOS-technologies was demonstrated [2], [3].

Commonly, there are three major approaches for building heterojunction bipolar transistors (HBTs) with an epitaxial SiGe or carbon-doped SiGe:C-base. The first two use nonselective epitaxy, where the extrinsic base is formed by the SiGe deposition itself. In some technologies, an additional polysilicon layer is used to lower the external base resistance [4], [5]. In this case, the extrinsic base can be highly doped by nonself-aligned (or quasi-self-aligned) implantation (see [6] and [7]) usually utilizing the structured emitter as an implantation mask. Due to tolerances especially in the alignment of the emitter lithography, the electrical link between the medium-doped intrinsic SiGe base and the heavily doped extrinsic base is not optimized, and thus, the base link resistance becomes rather high. Since the total base resistance, including this link, strongly influences the maximum oscillation frequency $f_{\max,\max}$, these types of transistors, although having the potential for very large values of $f_{t,\max}$, usually are not optimized with respect to $f_{\max,\max}$ [7].

As a second approach, also different self-alignment techniques can be applied in order to avoid these lithographical limitations and to achieve minimal base link resistance [8]–[11].

In the third approach, a variation of the widely used self-aligned double-poly concept for implanted-base transistors is employed. Here, the SiGe epitaxy is grown selectively, and base contact is established by vertical growth under a suspended base poly [3], [12]–[14]. Applying this double-poly concept, low extrinsic base resistances as well as low parasitic base-collector capacitancies can be achieved. However, the deposition and removal of the various additional dielectric and polysilicon layers make it rather complex and increase process costs. Similar arguments hold for the self-aligned nonselective technologies. The main technological challenge thereby lies in the subsequent etch steps that have to remove these sacrificial films from the MOS gates without leaving detrimental spacers. Here, we present a low complexity BiCMOS technology [quasi-single-poly technology (QSP)], comprising a selectively grown SiGe epitaxy, that utilizes the gate poly as a low resistivity base connect similar to [8] and [15]. Complex and expensive deposition of most additional dielectric films can be omitted which are obligatory in most conventional self-aligned concepts. The integration of the SiGe HBT requires five additional mask layers, when an epitaxial buried subcollector is used and only three additional mask layers when using a high-energy implanted buried layer (HE n-BL) [14]. Even though this concept strongly reduces process complexity in comparison to the conventional double-poly self-aligned process with a selectively grown SiGe base, the link resistance between the internal and the external base can be kept very low.

II. Integration

In Fig. 1 we compare the QSP integration scheme with our standard 0.25-μm BiCMOS process flow, as described in [16]. Two mask layers used for the definition of the sacrificial oxide in [16] can be saved with this integration scheme. Since no dedicated base poly is deposited for the QSP HBT, an additional mask layer has to be used to locally implant the gate-polysilicon

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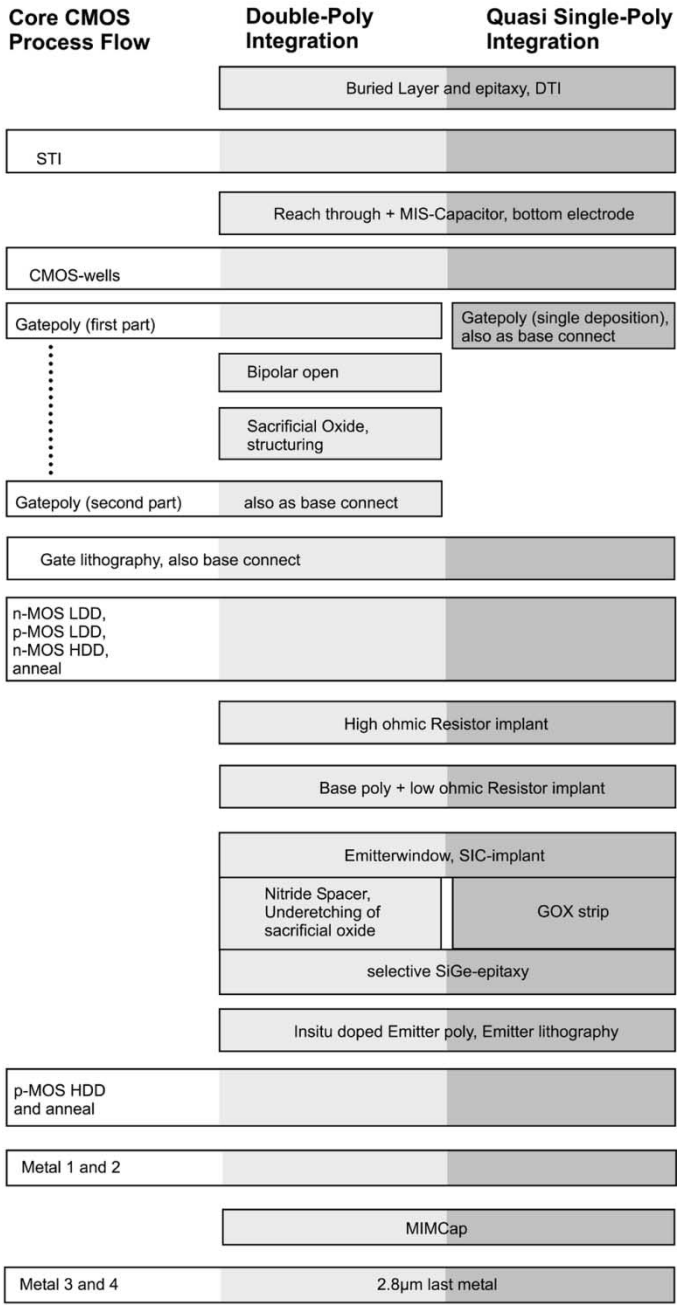

Fig. 1. Comparison of the process flows of our production double-poly BiCMOS integration concept with the quasi-single-poly concept.

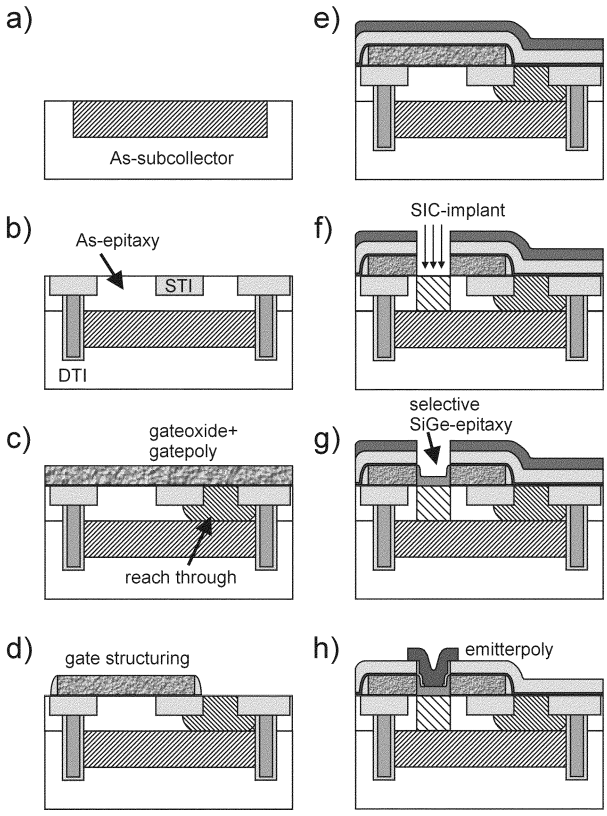

Fig. 2. Illustration of the HBT-fabrication: (a) As-subcollector formation, (b) epitaxy, DTI and STI formation, (c) reach through implantation and drive-in, gateoxide and-poly, (d) gate structuring, (e) isolation (f) emitter window, SIC-implant, (g) selectively grown SiGe epitaxy, and (h) emitter.

in the bipolar areas. Using a HE n-BL subcollector, this mask can simultaneously be employed to implant the buried layer, saving one mask layer in comparison to the epitaxial-collector concept.

In the following, the BiCMOS integration of the QSP concept is described in more detail. Starting from high-ohmic p-doped substrate (20 Ωcm), the buried subcollector of the HBT is conventionally formed by As implantation and furnace diffusion. In order to isolate individual p-wells, a low phosphorus-doped buried layer is formed by high energy implantation (>1 MeV) with an optimized rapid thermal anneal. Both layers are buried by deposition of a low n-doped epitaxial layer. The HBT fabrication is illustrated in Fig. 2. After a conventional poly- and oxide filled deep trench (DTI) for reduction of RF-crosstalk and a shallow trench process for lateral device isolation (STI), the highly phosphorus doped reach-through (or collector sinker) is implanted and diffused down to the buried subcollector. This mask layer can be omitted when using a HE n-BL. After implantation of the CMOS wells and the gate oxidation, the 250-nm-gate polylayer is deposited and structured. After the n-MOS lightly doped drain (LDD)-, highly doped drain (HDD)- and p-MOS LDD implants, the emitter isolation is deposited. An emitter window is etched through this isolation stack with the etching stopping on the gate oxide. At this stage of the process, the phosphorus doped self-aligned collector (SIC) is implanted and annealed. After gate oxide strip inside the emitter window, the selectively grown base of the SiGe HBT is deposited. The Ge content is linearly graded across the base to achieve an acceleration drift field for the electrons [12]. For the formation of an L-shaped oxide spacer inside the emitter window, that isolates emitter from base, we employ an auxiliary nitride layer. Care has to be spent on the spacer formation. A proper overetch of the nitride spacer is required to ensure a steep and reproducable spacer profile inside the emitter window (Fig. 3). In order to minimize the thermal budget in presence of the SiGe epitaxy, this layer is deposited by a rapid thermal chemical vapor deposition (RTCVD). As described above, the gate poly also serves as a base connect for the HBTs similar to [8]. In the BiCMOS-integration, it is also utilized as high- and low-ohmic poly resistors. Here, the base

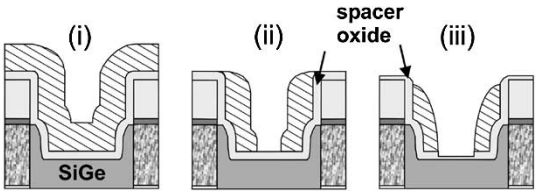

Fig. 3. Spacer formation includes (i) the deposition of an auxiliary nitride layer (striped) and (ii) a nitride etch to the underlying oxide. A proper overetch of the nitride spacer (iii) is required to ensure a steep and reproducable spacer profile inside the emitter window. The final oxide spacer is defined by wet oxide etching and nitride strip.

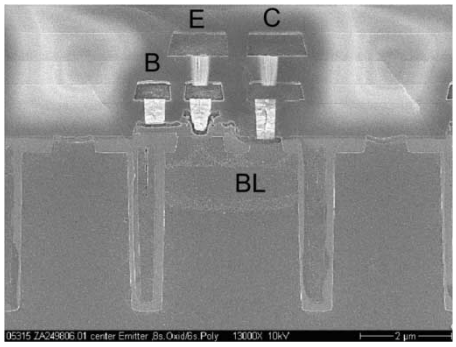

Fig. 4. Cross-sectional SEM micrograph of the self-aligned SiGe base bipolar transistor in a base(B)-emitter(E)-collector(C) arrangement. The buried layer is decorated to become visible.

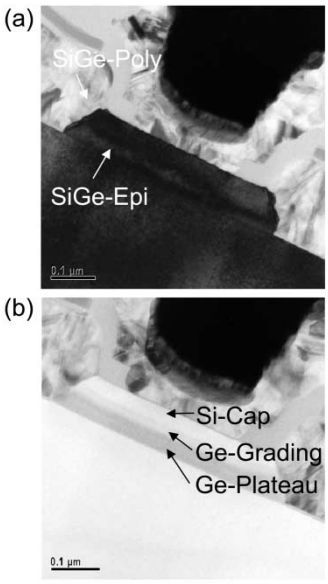

Fig. 5. (a) TEM close-up of the self-aligned SiGe base. (b) A tilted TEM image is shown, where the different epitaxial layers become clearly visible. The Si cap serves as the crystalline part of the emitter, the SiGe base consists of a SiGe grading and a SiGe plateau.

connect is simultaneously boron implanted with the low-ohmic poly resistors to save one more mask layer. In this case, for the HBT-module only four additional mask layers (epitaxial buried layer, reach through, emitter window and emitter poly) are necessary compared to the core CMOS process. Since the implanted base poly is exposed to a relatively high thermal budget, we believe that boron penetration through the gateoxide leads to a thin p-doped substrate layer beneath the base poly. Therefore, the extrinsic base is rather isolated from the collector by a pn junction than by the gateoxide. Finally, the emitter is diffused from an insitu As-doped polysilicon layer. Thus, the HBT is fabricated mainly in one block, separated from the CMOS core process. Only the final emitter drive-in is performed together with the p-HDD anneal. For an overview of the quasi-single-poly (QSP) HBT with shallow and deep trench isolation Fig. 4 shows a cross-sectional scanning electron microscope (SEM) micrograph. The highly As-doped epitaxial buried layer is decorated by wet etching for clarity.

The main difference between this integration scheme and the conventional concept is the growth and integration of the SiGe epitaxy. While in the conventional double-poly self-aligned concept, the epitaxy is connected to the base poly by vertical undergrowth beneath the poly using a sacrificial oxide, in the quasi-single-poly transistor the SiGe epitaxy is directly grown in the emitter window, leading to a polycrystalline lateral growth on the sidewalls of the gate poly, serving as base connect. As can be seen in the cross-sectional transmission electron microscope (TEM) micrographs in Fig. 5 the growth at the edges of the emitter window is without voids and the boundary of the poly- and monocrystalline regions is given by the (111)-crystallographic plane. Besides the low process complexity, one major advantage of this concept is the very short distance between the highly doped extrinsic base and the intrinsic SiGe base. Due to the texture of the gate poly, only a very thin (about 50 nm) SiGe poly is grown on the vertical edge of the base poly (see Fig. 5). This was also observed by Kondo *et al.* who used a similar HBT concept for a low-power bipolar technology [15]. Therefore only a very short/cold anneal is sufficient to diffuse boron from the base poly to the region under the L-spacer inside the emitter window to ensure excellent electrical contact. In contrast to other self-aligned SiGe technologies, where a nonselective epitaxy simultaneously serves as a base poly that is highly doped by implantation (e.g., [10]), no care has to be taken to avoid transient enhanced diffusion.

III. DC and AC Performance

In order to investigate the impact of the lateral base-link structure, we fabricated two types of quasi-single-poly HBTs and compared transistors of both types to those of the conventional type. For the first type, (in the following type A), the SiGe epitaxy was nominally grown identical to the conventional wafers. The collector-base breakdown voltage for both types of HBTs $\mathrm{BV_{CES}} \approx 11$ V for a 520-nm-thick collector epitaxy, similar to that of our conventional double-poly HBT. This indicates that collector-base breakdown mainly occurs in the SIC region, and is not considerably affected by the base link construction. In order to investigate the different contributions from the baselink and the internal base to the total base resistance $R_{B,\mathrm{tot}}$, for type B, the base doping was reduced. This mainly increased the internal base resistance $R_{B,\mathrm{int}}$. For both types of HBTs two effective emitter window widths ($w_{\mathrm{eff}} = 300$ nm and $w_{\mathrm{eff}} = 220$ nm) were available. In Table I, the most important electrical parameters of both types of the QSP-HBT are shown and compared to the SiGe HBT integrated with the conventional method. As

TABLE I
BIPOLAR KEY PARAMETERS OF BOTH TYPES OF QSP-HBTS AND OF THE CONVENTIONAL HBT, ALL OF THEM INTEGRATED IN A 0.25-μm BiCMOS TECHNOLOGY. J_C IS THE COLLECTOR CURRENT DENSITY

Quasi Single-Poly Selfaligned

	Type A		Type B	
eff. Emitter w_{eff}	300nm	220nm	300nm	220nm
$f_{t,max}$@ V_{CE}= 1V [GHz]	67	64	72	68
$f_{max,max}$(U)@ V_{CE}=1.0V [GHz] V_{CE}=2.5V [GHz]	108 159	118 184	99 150	108 163
$J_C(f_{max,max})$~ $J_C(f_{t,max})$ [mA/µm²] @V_{CE}=1.0V	1.8	2.0	1.7	2.1
BV_{CE0} [V]	2.6		2.5	
pinched base resistance [kΩ/sq]	5.7		8.1	

Double-Poly Selfaligned

eff. Emitter w_{eff}	420nm	340nm	260nm
$f_{t,max}$@ V_{CE}= 1V [GHz]	74	73	73
$f_{max,max}$(U)@ V_{CE}=1.0V [GHz] V_{CE}=2.5V [GHz]	99 137	110 154	118 165
$J_C(f_{max,max})$~ $J_C(f_{t,max})$ [mA/µm²] @V_{CE}=1.0V	1.7	1.7	1.9
BV_{CE0} [V]	2.5		
pinched base resistance [kΩ/sq]	~5.7		

can be seen, for the QSP-HBT type A, the maximum transit frequency $f_{t,\max}$ is slightly lower than for the conventional transistor with the same SiGe epitaxy. We believe that a nonoptimized SIC implantation for the QSP-HBT is responsible for the slightly reduced $f_{t,\max}$. However, taking typical lot to lot variations into account, the dc and ac parameters of both integration concepts are in good agreement. Type B with a somewhat shorter base width due to the lower doping displays the same $f_{t,\max}$ as the conventional HBT. The dc current amplification β is about 100 for type A and the conventional transistor and 130 for type B.

Also shown in Table I are the maximum oscillation frequencies extrapolated by the unilateral gain-method $f_{\max,\max}(U)$. Due to its lower base doping, and therefore increased base resistance $R_{B,\mathrm{tot}} = R_{B,\mathrm{int}} + R_{B,\mathrm{ext}}$, with $R_{B,\mathrm{ext}}$ being the external base or link resistance, $f_{\max,\max}(U)$ is lower for type B.

Fig. 6(a) and (b) exhibits the f_t traces, while Fig. 6 (c) and (d) shows the $f_{\max}(U)$ traces of the 220-nm HBT of type A and the 300-nm HBT of type B. Fig. 6(e) shows the unilateral gain U and Fig. 6(f) shows the current gain $h21$ of the QSP-HBT of type A and B respectively, measured up to a frequency of $f = 50$ GHz. For all frequencies between $f = 5$ and $f = 50$ GHz the -20 dB/dec gain roll-off as predicted by single-pole approximation is met with great accuracy. The values of $f_{t,\max}$ and $f_{\max,\max}$ shown in Table I are extrapolated to 0 dB from the point $f = 9.98$ GHz and $f = 31.55$ GHz, respectively, assuming the -20 dB/dec slope.

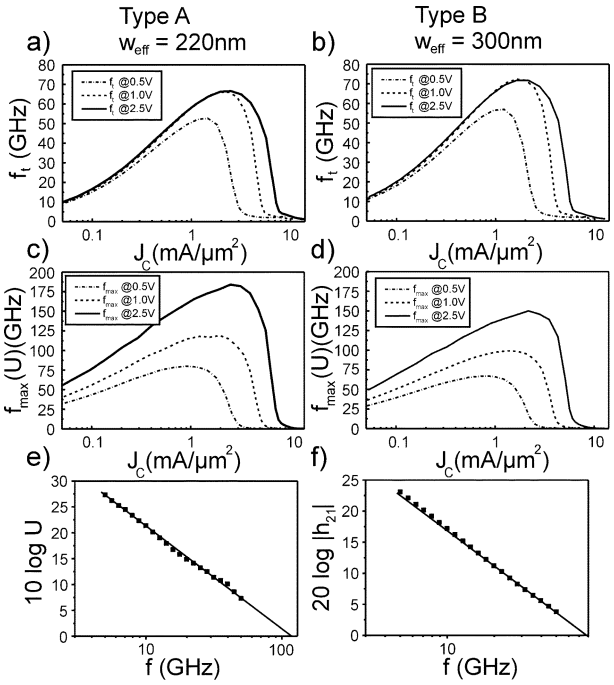

Fig. 6. (a), (b) f_t and (c), (d) $f_{\max}(U)$ for the type A and B transistor ($A_{\mathrm{eff}} = 0.22/0.30 \times 7.6\ \mu\mathrm{m}^2$) at different collector-emitter voltages. (e), (f) shows the extrapolation of $f_{t,\max}$ and $f_{\max,\max}(U)$ at $V_C = 1$ V for type A and B, respectively.

The maximum oscillation frequency $f_{\max,\max}$ can be deduced from $f_{t,\max}$, the base-collector capacitance C_{BC} and the base resistance $R_{B,\mathrm{tot}}$ using

$$f_{\max,\max} = \sqrt{\frac{f_{t,\max}}{8\pi R_{B,\mathrm{tot}} C_{\mathrm{BC}}}}. \tag{1}$$

As a good figure of merit for the quality of the HBT layout we therefore introduce $f^2_{\max,\max}/f_{t,\max}$, since this expression represents $R_{B,\mathrm{tot}}C_{\mathrm{BC}}$. In Fig. 7 a comparison is made between both types of QSP-HBTs and the conventional double-poly HBTs (see also Table I). Here, $f^2_{\max,\max}/f_{t,\max}$ is plotted against the effective emitter window width w_{eff}. The type A transistors lie on the same curve as the conventional HBTs. This indicates that for an identical intrinsic SiGe base and therefore identical $R_{B,\mathrm{int}}, R_{B,\mathrm{ext}} \times C_{\mathrm{BC}}$ is almost the same for both types of transistors.

The slopes in Fig. 7 are similar for all three types of transistors, supporting the assumption that the base link resistance of the quasi-single-poly HBT is similar to that of the well established double-poly self-aligned HBT. However, the quantitative derivation of $R_{B,\mathrm{ext}}$ from the slope of the curves in Fig. 7 lacks accuracy. First, a smaller emitter window causes a reduction of C_{BC} so that the slope in Fig. 7 does not solely represent $R_{B,\mathrm{tot}}$. Second, a smaller emitter window leads to an enhanced emitter perimeter depletion, meaning that the transistor behavior at the emitter perimeter deviates from that of the rest of the emitter [17].

A more reliable derivation of the external base resistance can be made by resistance measurements of the pinched base at different V_{BE} using transistor-like test structures with various emitter widths. The obtained resistance traces meet in one point

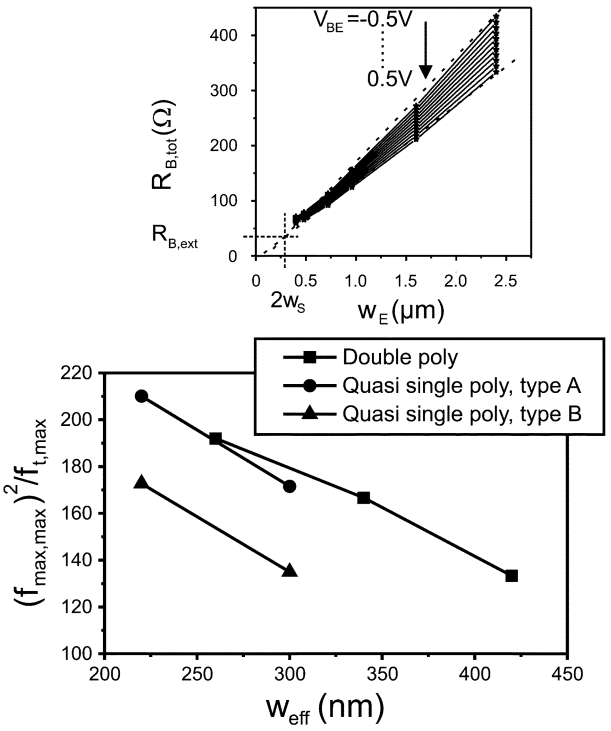

Fig. 7. $f_{\max,\max}(U)^2/f_{t,\max}$ versus effective emitter window width w_{eff} for both types of quasi-single-poly HBTs and also conventional double-poly HBTs for comparison. The upper inset shows $R_{B,\text{tot}}$ of a type A HBT as a function of V_{BE} for different w_E. This traces serve to derive $R_{B,\text{ext}}$ as described in [18].

indicating twice the spacer width w_S and the external base resistance $R_{B,\text{ext}}$ [18]. In our measurements shown in the upper inset in Fig. 7 this curves turned out to be nonlinear for small w_E, presumably caused by a smaller spacer width for decreasing w_E. Therefore, a more sophisticated evaluation of these measurements including averaging over many structures regarding only distinct pairs of emitter widths is needed. For the type A transistor, we derive a link resistance $R_{B,\text{ext}} = 418\ \Omega\mu$m, for type B $R_{B,\text{ext}} = 636\ \Omega\mu$m. For comparison, $R_{B,\text{ext}} = 243\ \Omega\mu$m for a conventional HBT, however, having a much shorter spacer length. Taking the differences in the spacer dimensions into account, the link resistance for the type A HBT is 15–25% higher in comparison to that of the double-poly self-aligned HBT. The type B transistors display an $R_{B,\text{ext}}$ about 50% higher than type A, being in good agreement with the difference in the internal base resistance $R_{B,\text{int}}$. This indicates that the laterally grown part of the SiGe base [indicated as SiGe poly in Fig. 5(a)] located between the spacer and the highly doped base poly influences $R_{B,\text{ext}}$. We assume that due to the columnar structure of the base poly, this region of the external SiGe base is less efficiently doped by lateral outdiffusion from the base poly and therefore $R_{B,\text{ext}}$ is slightly increased in comparison to the double-poly transistors.

To demonstrate the excellent dc-performance of the QSP-HBTs we show the Gummel plot and the dc-current gain β versus collector current for our $0.22 \times 1.20\ \mu\text{m}^2$ standard transistor of type A in Fig. 8. As can be seen, the current amplification β remains almost constant for about five decades of collector current (inset of Fig. 8) and the nonideal base current seen at low V_E is low. The variations in β are ≈10%

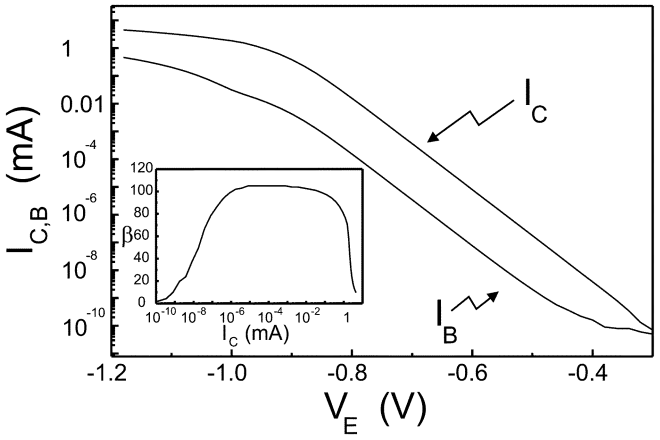

Fig. 8. Typical Gummel plot with corresponding current gain (inset) for a $0.22 \times 1.20\ \mu$m transistor of type A.

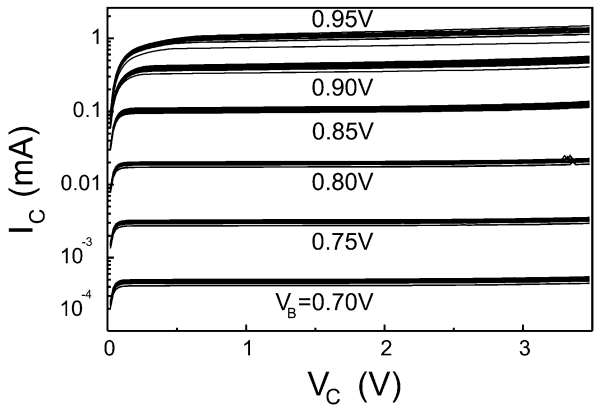

Fig. 9. Output characteristics for 16 HBTs of type A (effective emitter area $0.22 \times 1.20\ \mu$) at different base-emitter voltages V_B. At low collector currents an early voltage around -200 V can be deduced.

on a wafer. This value corresponds to $\Delta\beta/\beta$ for the reference double poly HBT. From the output characteristics for the HBT (type A) shown in Fig. 9 an early voltage $V_{\text{EA}} \approx -200$ V can be deduced at sufficiently low collector currents indicating excellent dc-performance especially important for the use in analog circuits. V_{EA} decreases at high collector currents due to self heating effects caused by the deep trench isolation structure surrounding the HBT.

The bipolar data presented here demonstrate balanced dc and ac performance well suitable for the design of wireless communication circuits.

The quarter micron core CMOS process is almost not affected by the integration of the QSP-HBT. In Fig. 10, the roll-off curves for both the n-MOS and the p-MOS transistors are shown. Especially the n-MOS hits the target for our conventional BiCMOS processes [16] very good. The p-MOS needs only a slight V_{th} adjust in order to fully meet our target spec.

Also, a fully functional single chip global system for mobile communication (GSM) quad-band transceiver with enhanced data rates for global evolution (EDGE) capability [16] has been realized using the QSP-BiCMOS integration concept presented here.

As a measure of bipolar transistor yield we evaluated the base-emitter (I_{BE}), collector-emitter (I_{CE}) and collector-base

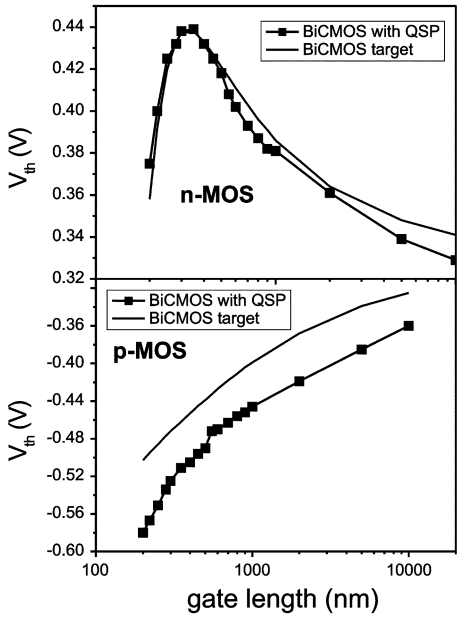

Fig. 10. Roll-off curves for both the n-MOS and the p-MOS transistors of the QSP-BiCMOS technology.

(I_{CB}) leakage currents with a yield criterion of $I \leq 1$ fA/μm^2 ($V_{\mathrm{CB}} = 2.5$ V, $V_{\mathrm{BE}} = 0.1$ V) for large multitransistors, each of them containing 3968 HBTs with an effective emitter area of 0.30×9.98 μm^2. The measurements were performed on a variety of wafers in a checkerboard arrangement with 29 dies on each wafer. The mean yield for a typical lot was found to be about 70% for all currents with a range up to 100% for the best wafers measured. The yield distribution across the wafer was homogeneous and comparable to wafers of the conventional double-poly process.

It is worth mentioning that the QSP concept is also suitable for further lateral shrinking and an upgrade to a SiGe:C-base [13]. The maximum allowed emitter stack height for a BiCMOS technology is decreasing with every further generation of the underlying core CMOS process. This makes the application of the conventional double-poly integration more and more difficult. The concept presented here eases this scaling limitation while maintaining the profits of the well established double-poly self-aligned SiGe integration with a selectively grown base.

IV. Conclusion

We presented a low-cost fully self-aligned integration concept for a SiGe HBT with a selectively grown base. The main feature was a selective epitaxial growth of the SiGe epitaxy using the gate poly as a lateral base connect. In comparison to a conventional double-poly integration concept, this approach significantly reduces process complexity. The dc and ac performance of the HBT equals the performance of a comparable conventional double-poly transistor.

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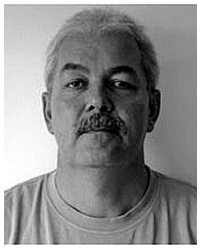

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