INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2006 UPDATE

TEST AND TEST EQUIPMENT

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TEST AND TEST EQUIPMENT

SUMMARY

The 2006 update to the ITRS Test Chapter is focused on minor corrections to previously published trend information. Corrections occurred to the Multi-Site wafer probing table where the parallelism for low performance microcontrollers was reduced. The Multi-Site efficiency numbers for the long-term years 2014 thru 2020 were omitted in the 2005 roadmap and have been included in the 2006 tables. NAND wafer and packaged unit test parallelism roadmap has been pulled in by 2 years and the NAND roadmap has been updated to reflect a higher bus performance starting in 2010. The system-oc-chip (SOC) roadmap reflects a push out of some defect models and analog test standards as progress in these areas have not kept up with the previous forecast. The mixed signal bandwidth and sampling rate roadmaps have been pulled in by a couple of years. This update does not identify any fundamental changes to the industry roadmap.

The 2005 roadmap did not contain the definitions of high, medium, or low "performance" for the various device types included in the tables. For the 2006 update, low end logic devices have fewer than 150 signal pins and an I/O bit rate of less than 400 Mbps. High performance Flash has an I/O bit rate of greater than 125 Mbps. The definition of performance is not static and should change over the duration of this roadmap. A table for high, medium, and low end performance will be further included in 2007 roadmap.

2007 international technology working group (ITWG) activities are focused on refining the full 2005 chapter rewrite and fleshing out areas that were not fully addressed. The rapid adoption of system-in-package (SIP), SOC, and NAND devices has been driving some trends faster than expected, which has resolved some difficult challenges but created others that will require new methodology such as testing SIP die "hidden" by other die.

Table 22 Summary of Key Test Drivers, Challenges, and Opportunities

KEY DRIVERS (NOT IN ANY PARTICULAR ORDER)	
Device trends	• Increasing device interface bandwidth (both number of signals and signal data rates) • Increasing device integration (SOC, SIP, MCP, 3D packaging) • Integration of emerging and non-digital CMOS technologies (RF, Analog, Optical, MEMs) • Package form factor and electrical / mechanical characteristics • Device characteristics beyond one sided deterministic stimulus/response model
Increasing test process complexity	• Increased device customization and line item complexity during the test process • Increasing "distributed test" to maintain cost scaling • Increased data feedback for tuning manufacturing • Higher order dimensionality of test conditions (e.g., adding multi-power, multi-voltage, multi-freq topologies to single valued T, V, freq)
Continued economic scaling of test	• Physical limits of further test parallelism • Managing (logic) test data volume • Effective limit for speed difference of HVM ATE versus DUT • Acceptable increases for interface hardware and (test) socket costs • Trade-off between the cost of test and the cost of quality
DIFFICULT CHALLENGES (IN ORDER OF PRIORITY)	
Test for yield learning	• Critically essential for fab process and device learning below optical device dimensions
Screening for reliability	• Increasing implementation challenges and efficacies of burn-in, IDDQ, and Vstress • Erratic, non deterministic, and intermittent device behavior
Increasing systemic defects	• Testing for local non-uniformities, not just hard defects • Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
Potential yield losses	• Tester inaccuracies (timing, voltage, current, temperature control, etc) • Overtesting (e.g., delay faults on non-functional paths) • Mechanical damage during the testing process • Defects occurring in test-only circuitry, e.g., BIST • Some IDDQ-only failures • Faulty repairs of normally repairable circuits • Overly aggressive statistical post-processing
FUTURE OPPORTUNITIES (NOT IN ANY ORDER)	
Test program automation (not ATPG)	Automation of generation entire test programs for ATEs
Simulation and modeling	Simulation and modeling of test interface hardware and instrumentation seamlessly integrated to the device design process
Convergence of test and system reliability solutions	Re-use and fungability of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMs—micro-electromechanical systems

Table 23a Multi-site Wafer Test (Package Test) for Product Segments—Near-term Years UPDATED

	Year of Production		*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm)		*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC ½ Pitch (nm)		*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	High Performance ASIC/MPU										
	Wafer test	Number of sites	8	8	8	16	16	16	16	32	32
		Multi-site efficiency [%]	95%	95%	95%	98%	98%	98%	98%	98%	98%
	Package test	Number of sites	4	4	4	8	8	8	8	16	16
IS		Multi-site efficiency [%]	92%	92%	92%	95%	95%	95%	95%	95%	95%
	Low Performance Microcontroller										
IS	Wafer test	Number of sites	16	16	32	64	64	64	64	64	64
IS	Wafer test	Multi-site efficiency [%]	90%	90%	95%	95%	95%	95%	95%	95%	95%
IS	Package test	Number of sites	8	16	32	64	64	64	64	64	64
IS	Package test	Multi-site efficiency [%]	85%	90%	95%	95%	95%	95%	95%	95%	95%
	Mixed-signal										
	Wafer test	Number of sites	4	4	4	8	8	16	16	16	16
IS		Multi-site efficiency [%]	85%	85%	85%	90%	90%	95%	95%	95%	95%
	Package test	Number of sites	4	8	8	16	16	16	16	16	64
IS		Multi-site efficiency [%]	85%	90%	90%	95%	95%	95%	95%	95%	95%
	*Commodity **DRAM** Memory*										
	Wafer test	Number of sites	128	256	512	512	1024 / Full wafer	1024 / Full wafer	1024 / Full wafer	1024 / Full wafer	1024 / Full wafer
IS		Multi-site efficiency [%]	75%	85%	90%	90%	90%	95%	95%	95%	95%
	Package test	Number of sites	128	256	256	512	512	1024	1024	1024	1024
IS		Multi-site efficiency [%]	90%	95%	95%	95%	95%	95%	95%	95%	95%
ADD	***Commodity Flash Memory***										
ADD	**Wafer test**	**Number of sites**	512	512	1024 / Full wafer	1024 / Full wafer	1024 / Full wafer	1024 / Full wafer	1024 / Full wafer	2048 / Wafer scale	2048 / Wafer scale
ADD	-	**Multi-site efficiency [%]**	95%	95%	95%	95%	95%	95%	95%	95%	95%
ADD	**Package test**	**Number of sites**	128	256	256	512	512	1024	1024	1024	1024
ADD	-	**Multi-site efficiency [%]**	90%	92%	95%	95%	95%	95%	95%	95%	95%
	RF										
	Wafer test	Number of sites	2	2	4	4	8	8	16	16	16
		Multi-site efficiency [%]	75%	75%	85%	85%	90%	90%	95%	95%	95%
	Package test	Number of sites	4	4	8	16	32	48	64	64	64
		Multi-site efficiency [%]	75%	90%	92%	95%	97%	97%	97%	97%	97%

Table 23b Multi-site Wafer Test (Package Test) for Product Segments—Long-term Years UPDATED

	Year of Production		*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm)		*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU/ASIC ½ Pitch (nm)		*28*	*25*	*22*	*20*	*18*	*16*	*14*
	High Performance ASIC/MPU								
	Wafer test	Number of sites	32	64	64	128	256	256	512 / Wafer scale
		Multi-site efficiency [%]	98%	98%	98%	98%	98%	98%	98%
	Package test	Number of sites	16	32	32	64	128	128	128
IS		Multi-site efficiency [%]	95%	95%	95%	95%	95%	95%	95%
	Low Performance Microcontroller								
IS	Wafer test	Number of sites	64	128	128	128	128	128	128
IS	Wafer test	Multi-site efficiency [%]	95%	95%	95%	95%	95%	95%	95%
IS	Package test	Number of sites	64	128	128	128	128	128	128
IS	Package test	Multi-site efficiency [%]	95%	95%	95%	95%	95%	95%	95%
	Mixed-signal								
	Wafer test	Number of sites	16	32	32	64	128	128	256
IS		Multi-site efficiency [%]	95%	95%	95%	95%	95%	95%	95%
	Package test	Number of sites	64	128	128	256	256	256	512
IS		Multi-site efficiency [%]	95%	95%	95%	95%	95%	95%	95%
	*Commodity **DRAM** Memory*								
	Wafer test	Number of sites	1024 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale
IS		Multi-site efficiency [%]	95%	95%	95%	95%	95%	95%	95%
	Package test	Number of sites	1024	2048	2048	2048	2048	2048	2048
IS		Multi-site efficiency [%]	95%	95%	95%	95%	95%	95%	95%
ADD	***Commodity Flash Memory***								
ADD	**Wafer test**	**Number of sites**	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale	2048 / Wafer scale
ADD	-	**Multi-site efficiency [%]**	95%	95%	95%	95%	95%	95%	95%
ADD	**Package test**	**Number of sites**	1024	2048	2048	2048	2048	2048	2048
ADD	-	**Multi-site efficiency [%]**	95%	95%	95%	95%	95%	95%	95%
	RF								
	Wafer test	Number of sites	32	32	32	64	128	128	256
		Multi-site efficiency [%]	95%	95%	95%	95%	95%	95%	95%
	Package test	Number of sites	128	128	128	256	256	256	512
		Multi-site efficiency [%]	97%	97%	97%	97%	97%	97%	97%

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

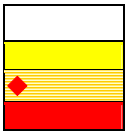

Table 24 SOC Model

			130 nm	90 nm	65 nm
Transistor Count (Million)	High Frequency Logic Part	Logic	4.7	7.1	10.9
		Memory	8.6	19.5	42.3
	Low Frequency Logic Part	Logic	6.8	10.3	15.7
		Memory	19.6	42.5	89.9
	Total		39.7	79.4	158.9

6 Test and Test Equipment

Table 25a System on Chip Test Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*35*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*85*	*76*	*67*	*60*	*54*	*48*	*42*	*38*	*34*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
	Embedded Cores									
IS	Standardization of Core Test Data [1]	Standard format on EDA/ATE			Extension to Analog Cores					
	Embedded Cores: Logic									
IS	Test Logic Insertion at RTL Design	Partially		Partially	Fully					
IS	Testability Analysis and Overhead Estimation at RTL Design	Ad hoc	Partially used	Partially used	Fully					
	BISR for Logic Cores	Minimal	Some						Logic BISR	
	Embedded Cores: Logic - Random Pattern Logic BIST									
	Area Investment beyond Scan (%) [2]	3.1	3.1	3.1	3.1	3.1	3.1	3.1	3.1	3.1
	Embedded Cores: Logic - Compressed Deterministic Pattern Test									
	Area Investment beyond Scan (%) [3]	1.1	1.2	1.3	1.4	1.5	1.6	1.6	1.7	1.8
	Test Pattern Length (Number of Captures) [4]	1.0	1.3	1.6	2.0	2.5	3.2	4	5	6
	Test Pattern Length Compression Ratio [5]	1.0	1.4	2.0	3.1	5.2	9.2	18	23	30
	Test Data Volume Compression Ratio [6]	100	120	150	210	300	460	770	860	980
	Embedded Cores: Memory									
IS	Area Investment of SRAM BIST/BISR (Kgates/Mbits)	35	35	35	35	35	35	35	35	35
	Repairing Mechanism of Embedded SRAM Cells [7]	BISR		BISR for Row & Col R/D					BISR for More Sophisticated R/D	
	Embedded Cores: Analog									
	DFT (BIST, BOST) for Analog Cores	Limited use (PLL, ADC, etc.)				Partial				
	Design for Failure Analysis of Analog Cores	Ad hoc								
	Core Access									
	Use of Standard Interface on IP Core Access	Partially								
	Analog-Mixed Signal Core Access	Direct Access				Analog wrapper [8]			Standard analog wrapper [8]	
	SoC Level Testing									
	Test Strategy for IP Core-Based Design [9]	Partially automated			Fully automated					
	DFT Selection for Cores	DFT selection for cores			Selection for cores/fully automated EDA tool					
IS	DFT at Higher Level Design [10]	No			Partially	Partially	Partially	Yes	Yes	Yes
	Fault Model for SoC									
IS	Test quality model for SoC Level defect Coverage [11]	fault models for each core				New method, its coverage [12]				
	Delay Fault Model with High Accuracy	Partially	Partially	Fully usable						
IS	X-talk Fault Model	No			No	Partially	Fully usable			
	Manufacturing									
IS	Diagnosis Interface/Data [13]	Standard format and methods on IP core			Standard format and methods on IP core	Automated SoC diagnosis				

BOST—built off-chip self test *BISR—built-in self repair*

Table 25b System on Chip Test Requirements—Long-term Years UPDATED

	Year of Production	2014	2015	2016	2017	2018	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	30	27	24	21	19	17	15
	MPU Physical Gate Length (nm)	11	10	9	8	7	6	6
	Embedded Cores							
IS	Standardization of Core Test Data [1]	Extension to Analog Cores						
	Embedded Cores: Logic							
IS	Test Logic Insertion at RTL Design	Fully						
IS	Testability Analysis and Overhead Estimation at RTL Design	Fully						
	BISR for Logic Cores	Logic BISR						
	Embedded Cores: Logic - Random Pattern Logic BIST							
	Area Investment beyond Scan (%) [2]	3.1	3.1	3.1	3.1	3.1	3.1	3.1
	Embedded Cores: Logic - Compressed Deterministic Pattern Test							
	Area Investment beyond Scan (%) [3]	1.9	2	2.1	2.1	2.1	2.1	2.1
	Test Pattern Length (Number of Captures) [4]	8	10	13	16	20	25	32
	Test Pattern Length Compression Ratio [5]	40	55	68	83	100	130	160
	Test Data Volume Compression Ratio [6]	1,140	1,360	1,450	1,560	1,680	1,810	1,960
	Embedded Cores: Memory							
IS	Area Investment of SRAM BIST/BISR (Kgates/Mbits)	35	35	35	35	35	35	35
	Repairing Mechanism of Embedded SRAM Cells [7]	BISR for More Sophisticated R/D						
	Embedded Cores: Analog							
	DFT (BIST, BOST) for Analog Cores	Partial				Full use		
	Design for Failure Analysis of Analog Cores	Partially structural	Structural					
	Core Access							
	Use of Standard Interface on IP Core Access	Partially	Fully					
	Analog-Mixed Signal Core Access	Standard analog wrapper [8]						
	SoC Level Testing							
	Test Strategy for IP Core-Based Design [9]	Fully automated						
	DFT Selection for Cores	Selection for cores/fully automated EDA tool						
IS	DFT at Higher Level Design [10]	Yes						
	Fault Model for SoC							
IS	Test quality model for SoC Level defect Coverage [11]	New method, its coverage [12]						
	Delay Fault Model with High Accuracy	Fully usable						
IS	X-talk Fault Model	Fully usable						
	Manufacturing							
IS	Diagnosis Interface/Data [13]	Automated SoC diagnosis						

Manufacturable solutions exist, and are being optimized
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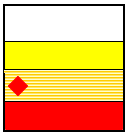

8 Test and Test Equipment

Definitions for Tables 25a and b:

[1] The standardization of test data format needs to reduce turn-around-time of test program development

[2] Area investment of random pattern logic BIST consists of BIST controller and test points.

[3] Area investment of compressed deterministic pattern test logic consists of controller and test points.

[4] Required number of test pattern length (number of captures), which is normalized based on the number on 2005.

[5] Test pattern compression ratios are values which are necessary to suppress the total test pattern length (sum of those for stuck-at, transition, path delay and X-talk tests) in the table within the required test pattern length.

[6] Ratio of compressed test data volume in the tester memory against conventional scan test data volume with same fault coverage

[7] Hard repair which uses optical or electrical fuse devices for the programming

[8] Extended wrapper structure to access to embedded analog-MS cores, not chip-level analog boundary-scan

[9] The strategy contains test control integration, test scheduling for low power consumption, test time and test pin reduction

IS *[10] High-level synthesis with testability analysis for scan or Instruction-based test*

IS *[11] The standard menu of fault models and coverage is required to popularize IP Cores*

[12] A method to obtain overall test quality measure of SoC considering all embedded devices; logic, memory and analog.

IS *[13] The standardization of diagnosis data format and interface (Independent of DFT and ATE) is required to reduce turn-around-time of failure analysis*

Table 26a Logic Test Requirements—Near-term Years

Year of Production		*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)		*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)		*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)		*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Part 1: High Volume Microprocessor Trends Drivers										
Functions per chip at production (million transistors [Mtransistors])		**193**	**193**	**386**	**386**	**386**	**773**	**773**	**773**	**1,546**
Chip size at production (mm^2)		**111**	**88**	**140**	**111**	**88**	**140**	**111**	**88**	**140**
Number of processor cores		**2**	**2**	**4**	**4**	**4**	**8**	**8**	**8**	**16**
Nominal V_{dd} Range (V)		**0.9–1.1**	**0.9–1.1**	**0.8–1.1**	**0.8–1.0**	**0.8–1.0**	**0.7–1.0**	**0.7–1.0**	**0.7–0.9**	**0.6–0.9**
Chip-to-board (off-chip) speed (high-performance, for peripheral buses) (MHz)		**3125**	**3906**	**4883**	**6103**	**7629**	**9536**	**TBD**	**14901**	**18626**
Part 2: High Volume Microprocessor Test Requirements										
I/O data rate (GT/s)		**0.1 - 3**	**0.1 - 6**	**0.1 - 6**	**0.1 - 6**	**0.2 - 12**	**0.2 - 12**	**0.2 - 12**	**0.2 - 15**	**0.2 - 15**
I/O types		**Slow speed scan / DFT, source synchronous, clock forwarding, clock embedded**				**Slow speed scan / DFT, clock forwarded, clock embedded**				
Total device maximum power consumption at test (W)	Client	**200**	**200**	**200**	**200**	**300**	**300**	**300**	**300**	**300**
	Server	**200**	**250**	**300**	**300**	**300**	**300**	**300**	**300**	**300**
Number of power supplies per site		**1–4**	**1–4**	**1–6**	**1–6**	**1–6**	**1–4**	**1–4**	**1–3**	**1–3**
Power supplies voltage range (V)		**0.7–2.0**	**0.7–2.0**	**0.6–2.0**	**0.6–2.0**	**0.6–2.0**	**0.6–12**	**0.6–12**	**0.6–12**	**0.6–12**
Scan vector memory (Mbit per pin)		**64-256**	**64-256**	**64-256**	**64-256**	**64-512**	**64-512**	**64-512**	**64-512**	**64-1024**
Functional vector memory (M-vectors per pin)		**16-128**	**16-128**	**16-128**	**16-128**	**16-256**	**16-256**	**16-256**	**16-256**	**16-512**

Values for the year 2011 will be determined in the 2006 ITRS Update.

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

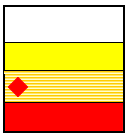

Table 26b Logic Test Requirements—Long-term Years

Year of Production		*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)		*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)		*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)		*11*	*10*	*9*	*8*	*7*	*6*	*6*
Part 1: High Volume Microprocessor Trends Drivers								
Functions per chip at production (million transistors [Mtransistors])		**1,546**	**1,546**	**3,092**	**3,092**	**3,092**	**6,184**	**6,184**
Chip size at production (mm^2)		**111**	**88**	**140**	**111**	**88**	**140**	**111**
Number of processor cores		**16**	**16**	**32**	**32**	**32**	**64**	**64**
Nominal Vdd Range (V)		**0.6–0.9**	**0.6–0.8**	**0.5–0.8**	**0.5–0.7**	**0.5–0.7**	**0.4–0.7**	**0.4–0.6**
Chip-to-board (off-chip) speed (high-performance, for peripheral buses) (MHz)		**TBD**	**29103**	**36379**	**TBD**	**56843**	**TBD**	**TBD**
Part 2: High Volume Microprocessor Test Requirements								
I/O data rate (GT/s)		**0.2-20**	**0.2-20**	**0.2-20**	**0.2-40**	**0.2-40**	**0.2-40**	**0.2-40**
I/O types		**Slow speed scan / DFT, advanced clock embedded, optical**						
Total device maximum power consumption at test (W)	Client	**300**	**300**	**300**	**300**	**300**	**300**	**300**
	Server	**400**	**400**	**400**	**400**	**400**	**400**	**400**
Number of power supplies per site		**1–3**	**1–3**	**1–3**	**1–3**	**1–3**	**1–3**	**1–3**
Power supplies voltage range (V)		**0.6–12**	**0.6–12**	**0.6–48**	**0.6–48**	**0.6–48**	**0.6–48**	**0.6–48**
Scan vector memory (Mbit per pin)		**64–1024**	**64–1024**	**64–1024**	**64–1024**	**64–1024**	**64–1024**	**64–1024**
Functional vector memory (M-vectors per pin)		**16–512**	**16–512**	**16–512**	**16–1024**	**16–1024**	**16–1024**	**16–1024**

Values for the years 2014, 2017, 2019, and 2020 will be determined in the 2006 ITRS Update.

Manufacturable solutions exist, and are being optimized
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Manufacturable solutions are NOT known

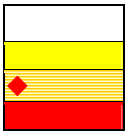


Table 27a Commodity DRAM Test Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	DRAM Capacity (Gbits)									
	R&D	8	8	16	16	16	32	32	32	64
	Mass production	1	2	2	2	4	4	4	8	8
	DRAM data rate (Gbs)	0.67	0.80	1.00	1.20	1.20	1.33	1.33	1.50	1.50
	Performance DRAM data rate (Gbs)	1.8	2.25	2.5	3	3.5	5	5	6	6
	DRAM bit width/device (mass production)	16	16	16	16	16	16	16	16	16
	Device CLK rate (GHz)	0.3	0.3	0.4	0.5	0.5	0.6	0.7	0.7	0.8
IS	Overall timing accuracy (ps)	40	40	32	32	25	25	25	CBD	

CLK—clock signal ***CBD—cannot be determined***

Table 27b Commodity DRAM Test Requirements—Long-term Years UPDATED

	Year of Production	2014	**2015**	2016	2017	**2018**	2019	2020
	DRAM ½ Pitch (nm) (contacted)	28	25	22	20	18	16	14
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	28	25	22	20	18	16	14
	DRAM Capacity (Gbits)							
	R&D	64	64	128	128	128	256	256
	Mass production	8	16	16	16	32	32	32
	DRAM data rate (Gbs)	1.8	1.8	2.0	2.0	2.25	2.25	2.5
	Performance DRAM data rate (Gbs)	8	8	10	10	12	12	14
	DRAM bit width/device (mass production)	16	16	16	16	16	16	16
	Device CLK rate (GHz)	0.9	0.9	1.0	1.1	1.1	1.2	1.3
IS	Overall timing accuracy (ps)	CBD						

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

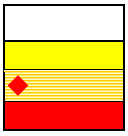


Table 28a Commodity Flash Memory Test Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
	NAND Device Characteristics									
	Capacity (Gbits)									
	R&D	32	32	64	64	128	128	128	256	256
	Mass production	8	8	16	16	32	32	32	64	64
	Data width (bits)	16	16	16	16	16	16	16	16	16
	Power Supplies									
	Power supply voltage range	1.5–5.5	1.5–5.5	1.5–5.5	1.5–3.5	1.5–3.5	1.5–3.5	1.5–3.5	1.5–3.5	1.5–3.5
	Power supplies per device	2	2	2	2	2	2	2	2	2
	Maximum current (MA)	35	35	35	35	35	35	35	35	35
	Pattern Generator									
	Tester channels per device	24	24	24	24	24	24	24	24	24
	Timing									
IS	Maximum I/O data rate (Mbs)	40	40	50	50	50	66	66	100	100
IS	Accuracy OTA (ns)	1.2	1.2	1	1	1	0.8	0.8	0.5	0.5
	NOR Device Characteristics									
	Capacity (Gbits)									
	R&D	4	4	8	8	16	16	16	32	32
	Mass production	1	1	2	2	4	4	4	8	8
	Data width (bits)	16	16	16	32	32	32	32	32	32
	Power supply voltage range	1.0–5.5	1.0–5.5	1.0–5.5	1.0–5.5	0.9–3.3	0.9–3.3	0.9–3.3	0.9–3.3	0.9–3.3
	Power supplies per device***	2	2	2	2	2	2	2	2	2
	Maximum current (MA)	150	150	150	150	150	150	150	150	150
	Tester channels per test site	64	72	72	72	72	72	72	72	72
	Maximum I/O data rate (Mbs)	166	200	200	200	266	266	266	333	333
	Accuracy OTA (ns)	0.3	0.2	0.2	0.2	0.18	0.18	0.18	0.15	0.15

OTA—overall ATE timing accuracy

**** Discrete only*

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

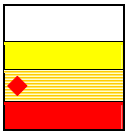


Table 28b Commodity Flash Memory Test Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	NAND Device Characteristics							
	Capacity (Gbits)							
	R&D	**256**	**512**	**512**	**512**	**1024**	**1024**	**1024**
	Mass production	**64**	**128**	**128**	**128**	**256**	**256**	**256**
	Data width (bits)	**16**	**16**	**16**	**16**	**16**	**16**	**16**
	Power Supplies							
	Power supply voltage range	**1.5–3.5**	**1.5–3.5**	**1.5–3.5**	**1.5–3.5**	**1.5–3.5**	**1.5–3.5**	**1.5–3.5**
	Power supplies per device	**2**	**2**	**2**	**2**	**2**	**2**	**2**
	Maximum current (MA)	**35**	**35**	**35**	**35**	**35**	**35**	**35**
	Pattern Generator							
	Tester channels per device	**24**	**24**	**24**	**24**	**24**	**24**	**24**
	Timing							
IS	Maximum I/O data rate (Mbs)	**100**	**100**	**133**	**133**	**133**	**133**	**133**
IS	Accuracy OTA (ns)	**0.5**	**0.5**	**0.4**	**0.4**	**0.4**	**0.4**	**0.4**
	NOR Device Characteristics							
	Capacity (Gbits)							
	R&D	**32**	**64**	**64**	**64**	**128**	**128**	**128**
	Mass production	**8**	**16**	**16**	**16**	**32**	**32**	**32**
	Data width (bits)	**32**	**32**	**32**	**32**	**32**	**32**	**32**
	Power supply voltage range	**0.9–3.3**	**0.9–3.3**	**0.9–3.3**	**0.9–3.3**	**0.9–3.3**	**0.9–3.3**	**0.9–3.3**
	Power supplies per device***	**2**	**2**	**2**	**2**	**2**	**2**	**2**
	Maximum current (MA)	**150**	**150**	**150**	**150**	**150**	**150**	**150**
	Tester channels per test site	**72**	**72**	**72**	**72**	**72**	**72**	**72**
	Maximum I/O data rate (Mbs)	**333**	**400**	**400**	**400**	**400**	**400**	**400**
	Accuracy OTA (ns)	**0.15**	**0.12**	**0.12**	**0.12**	**0.12**	**0.12**	**0.12**

*** *Discrete only*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

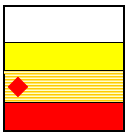


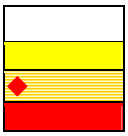
Table 29a Embedded Memory (DRAM and Flash) Test Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
Embedded DRAM									
Embedded DRAM size (Mbits) *									
R&D	**256**	**512**	**512**	**512**	**1024**	**1024**	**1024**	**2048**	**2048**
Mass production	**128**	**256**	**256**	**256**	**512**	**512**	**512**	**1024**	**1024**
Failure concerns	**Particle defects; array noise, data retention**					**Particle defects, array noise, sense-amp imbalance**			
Wafer level test	**Single and double insertion**					**In-line defect detection**			
Usage of on-chip test	**100% BIST/BISR**					**100% BIST/100% BISR**			
Embedded Flash									
Embedded flash size (Mbits) *									
R&D	**64**	**128**	**128**	**128**	**256**	**256**	**256**	**512**	**512**
Mass production	**32**	**64**	**64**	**64**	**128**	**128**	**128**	**256**	**256**
Embedded mixed memory size (Mbits) *									
Flash	**32**	**64**	**64**	**64**	**128**	**128**	**128**	**256**	**256**
DRAM	**32**	**64**	**64**	**64**	**128**	**128**	**128**	**256**	**256**
Failure concerns	**Oxide defects; ONO scaling; over-erase**					**Sense-amp imbalance**			
Wafer level test	**Single and double insertion**					**In-line defect detection**			
Usage of on-chip test	**BIST/BIST/DAT**					**BIST/BISR**			

DAT—direct access DFT

Number of bits in mass production is approximately 50% of number of bits in R&D

** Solution space is both on-chip and stacked die*



Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

Table 29b Embedded Memory (DRAM and Flash) Test Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
Embedded DRAM							
Embedded DRAM size (Mbits)							
R&D	**2048**	**4096**	**4096**	**4096**	**8184**	**8192**	**8192**
Mass production	**1024**	**2048**	**2048**	**2048**	**4092**	**4096**	**4096**
Failure concerns	**Particle defects, array noise, sense-amp imbalance**						
Wafer level test	**In-line defect detection**						
Usage of on-chip test	**100% BIST/100% BISR**						
Embedded Flash							
Embedded flash size (Mbits)							
R&D	**512**	**1024**	**1024**	**1024**	**2046**	**2048**	**2048**
Mass production	**256**	**512**	**512**	**512**	**1023**	**1024**	**1024**
Embedded mixed memory size (Mbits)							
Flash	**256**	**512**	**512**	**512**	**1023**	**1024**	**1024**
DRAM	**256**	**512**	**512**	**512**	**1023**	**1024**	**1024**
Failure concerns	**Sense-amp imbalance**						
Wafer level test	**In-line defect detection**						
Usage of on-chip test	**BIST/BISR**						

* *Solution space is both on-chip and stacked die*

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

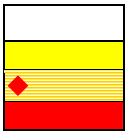


Table 30a Mixed-signal Test Requirements—Near-term Years UPDATED

	Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
	DRAM ½ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32	28
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32	90
	MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13	11
	Low Frequency Waveform										
	BW (MHz)	50	50	50	75	75	75	100	100	100	100
	Sample rate (MS/s)	Moving from Nyquist sample rates to over/under sampling sources/digitizers									
	Resolution (bits)	DSP computation to 24 bits – however effective number of bits will be limited by noise fllor									
	Noise floor (dB/RT Hz)	-155	-155	-155	-160	-160	-160	-165	-165	-165	-165
	Very High Frequency Waveform Source										
	Level V (pk–pk)	4	4	4	4	Driven by communication physical layer standards – likely to be lower					
	Accuracy (±)	0.50%	0.50%	0.50%	0.50%	Likely to remain the same					
IS	BW (MHz)	1500	1500	1600	1900	2250	2700	2700	3000	3000	3000
IS	Sample rate (MS/s)	6000	6000	6400	7600	9000	10,800	10,800	12000	12000	12000
IS	Resolution (bits) AWG/Sine†	8/10	8/10	8/10	8/10	8/10	8/10	8/10	10/12	10/12	10/12
IS	Noise floor (dB/RT Hz)	-135	-135	-140	-140	-140	-140	-140	-145	-145	-145
	Very High Frequency Waveform Digitizer										
	Level V (pk–pk)	4	4	4	4	Driven by communication physical layer standards – likely to be lower					
	Accuracy (±)	0.50%	0.50%	0.50%	0.50%	Likely to remain the same					
	BW (MHz) (undersampled)	6400	8000	9200	10800	10800	12500	12500	15000	15000	15000
	Sample rate (MS/s)	Direct conversion <400 MS/s							Direct conversion <600 MS/s		
	Resolution (bits)	Minimum 12 bits – noise floor is more important							Minimum 14 bits – noise floor is more important		
	Noise floor (dB/RT Hz)	-145	-145	-145	-145	-145	-145	-145	-150	-150	-150
	Time Measurement										
	Jitter measurement (ps RMS)	Will be driven by high-speed serial communication ports									
	Frequency measurement (MHz)	Will be driven by high-performance ASIC clock rates									
	Single shot time capability (ps)	Will be driven by high-speed serial communication ports									
	RF/Microwave instrumentation	Same as RF test requirements – see this new section									
	Special Digital Capabilities										
	D/A and A/D digital data rate (MB/s)	Same as high performance ASIC "off-chip data rate"									
	Sample clock jitter (ps RMS)	<0.2	<0.2	<0.2	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1	<0.1

AWG—array waveguide gratings BW—bandwidth pk–pk—peak to peak

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

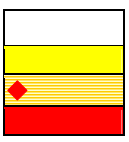
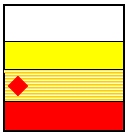


Table 30b Mixed-signal Test Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
	Low Frequency Waveform							
	BW (MHz)	**100**	**100**	**100**	**100**	**100**	**100**	**100**
	Sample rate (MS/s)	**Moving from Nyquist sample rates to over/under sampling sources/digitizers**						
	Resolution (bits)	**DSP computation to 24 bits – however effective number of bits will be limited by noise fllor**						
	Noise floor (dB/RT Hz)	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**	**-165**
	Very High Frequency Waveform Source							
	Level V (pk–pk)	**Driven by communication physical layer standards – likely to be lower**						
	Accuracy (±)	**Likely to remain the same**						
IS	BW (MHz)	**3750**	**3750**	**3750**	**3750**	**3750**	**3750**	**3750**
IS	Sample rate (MS/s)	**15000**	**15000**	**15000**	**15000**	**15000**	**15000**	**15000**
IS	Resolution (bits) AWG/Sine†	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**	**10/12**
	Noise floor (dB/RT Hz)	**-145**	**-145**	**-145**	**-145**	**-145**	**-144**	**-143**
	Very High Frequency Waveform Digitizer							
	Level V (pk–pk)	**Driven by communication physical layer standards – likely to be lower**						
	Accuracy (±)	**Likely to remain the same**						
	BW (MHz) (undersampled)	**15000**	**15000**	**15000**	**15000**	**15000**	**15000**	**15000**
	Sample rate (MS/s)	**Direct conversion <600 MS/s**						
	Resolution (bits)	**Minimum 14 bits – noise floor is more important**						
	Noise floor (dB/RT Hz)	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**	**-150**
	Time Measurement							
	Jitter measurement (ps RMS)	**Will be driven by high-speed serial communication ports**						
	Frequency measurement (MHz)	**Will be driven by high-performance ASIC clock rates**						
	Single shot time capability (ps)	**Will be driven by hihg-speed serial communication ports**						
	RF/Microwave instrumentation	**Same as RF test requirements – see this new section**						
	Special Digital Capabilities							
	D/A and A/D digital data rate (MB/s)	**Same as high performance ASIC "off-chip data rate"**						
	Sample clock jitter (ps RMS)	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**	**<0.1**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Definitions for Mixed-signal Test Requirements Table 30:
Low Frequency Source and Digitizer—This is the basic, minimum, instrument set of any mixed-signal tester. Telecommunications, advanced audio and wireless baseband will drive these specifications. Differential inputs/outputs are required.
Very High Frequency Waveform Source—Disk storage applications will drive sample rate and bandwidth. Local area network devices will drive sample rate, resolution and amplitude accuracy. Differential outputs are required.
Very High Frequency Waveform Digitizer—Undersampled (down conversion, track-and-hold, etc) bandwidth is shown. The sample rates and bit resolutions are for a direct conversion digitizer, which is usually preceded by the undersampler. Storage and network devices will drive digitizer specifications. Differential inputs are required.
Special Digital Capabilities—For converter testing, the ability to source a digital signal to a D/A and capture a digital signal from an A/D.

Table 31a Burn-in Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**	**75**	**75**	**75**
Power dissipation (W per DUT)	**600**	**600**	**600**	**600**	**600**	**600**	**600**	**600**	**600**
Power Supply Voltage Range (V)									
High-performance ASIC / microprocessor / graphics processor	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5-2.5**	**0.5–2.5**	**0.5–2.5**
Low-end microcontroller	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**	**0.7–10.0**	**0.5–10**	**0.5–10**	**0.5–10**	**0.5–10**
Mixed-signal	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–500**	**0.5–500**
Maximum Number of Signal I/O									
High-performance ASIC	**384**	**384**	**384**	**384**	**384**	**384**	**384**	**384**	**384**
High-performance microprocessor / graphics processor / mixed-signal	**128**	**128**	**128**	**128**	**128**	**128**	**128**	**128**	**128**
Commodity memory	**72**	**72**	**72**	**72**	**72**	**72**	**72**	**72**	**72**
Maximum Current (A)									
High-performance microprocessor	**400**	**450**	**450**	**450**	**450**	**450**	**450**	**450**	**450**
High-performance graphics processor	**40**	**80**	**100**	**150**	**200**	**200**	**200**	**200**	**200**
Mixed-signal	**20**	**20**	**20**	**20**	**20**	**30**	**30**	**30**	**30**
Burn-in Socket									
Pin count	**2500**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**
Pitch (mm)	**0.4**	**0.4**	**0.3**	**0.3**	**0.3**	**0.2**	**0.2**	**0.2**	**0.2**
Power consumption (A/Pin)	**2.0**	**3.0**	**3.0**	**4.0**	**4.0**	**5.0**	**5.0**	**5.0**	**5.0**
Wafer Level Burn-In									
Maximum burn-in temperature (ºC)	**150±3**	**150±3**	**175±3**	**175±3**	**175±3**	**175±3**	**175±3**	**175±3**	**175±3**
Pad Layout – Linear									
Minimum pad pitch (µm)	**80**	**80**	**65**	**65**	**65**	**65**	**65**	**65**	**65**
Minimum pad size (µm)	**60**	**60**	**50**	**50**	**50**	**50**	**50**	**50**	**50**
Maximum number of probes	**70k**	**70k**	**70k**	**70k**	**70k**	**70k**	**70k**	**70k**	**70k**
Pad Layout – Periphery, Area Array									
Minimum pad pitch (µm) *1	**100**	**100**	**100**	**80**	**80**	**80**	**80**	**80**	**80**
Minimum pad size (µm)	**45**	**40**	**40**	**35**	**35**	**35**	**35**	**30**	**30**
Maximum number of probes	**125k**	**125k**	**150k**	**150k**	**150k**	**150k**	**150k**	**150k**	**150k**
Power consumption (W/DUT – Low-end microcontroller, DFT/BIST SOC *2)	**10**	**10**	**10**	**10**	**10**	**20**	**20**	**20**	**20**
Vector memory depth (M vectors – DFT/BIST SOC *2)	**16**	**32**	**32**	**64**	**64**	**64**	**64**	**64**	**64**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

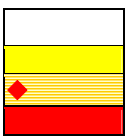


Table 31b Burn-in Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Clock input frequency (MHz)	**400**	**400**	**400**	**400**	**400**	**400**	**400**
Off-chip data frequency (MHz)	**75**	**75**	**75**	**75**	**75**	**75**	**75**
Power dissipation (W per DUT)	**600**	**600**	**600**	**600**	**600**	**600**	**600**
Power Supply Voltage Range (V)							
High-performance ASIC / microprocessor / graphics processor	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.5–2.5**	**0.4–2.5**	**0.4–2.5**	**0.4–2.5**
Low-end microcontroller	**0.5–10**	**0.5–10**	**0.5–10**	**0.5–10**	**0.5–10**	**0.5–10**	**0.5–10**
Mixed-signal	**0.5–500**	**0.5–1000**	**0.5–1000**	**0.5–1000**	**0.5–1000**	**0.5–1000**	**0.5–1000**
Maximum Number of Signal I/O							
High-performance ASIC	**384**	**384**	**384**	**384**	**384**	**384**	**384**
High-performance microprocessor / graphics processor / mixed-signal	**128**	**128**	**128**	**128**	**128**	**128**	**128**
Commodity memory	**72**	**72**	**72**	**72**	**72**	**72**	**72**
Maximum Current (A)							
High-performance microprocessor	**450**	**450**	**450**	**450**	**450**	**450**	**450**
High-performance graphics processor	**200**	**200**	**200**	**200**	**200**	**200**	**200**
Mixed-signal	**30**	**30**	**30**	**30**	**30**	**30**	**30**
Burn-in Socket							
Pin count	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**	**3000**
Pitch (mm)	**0.2**	**0.1**	**0.1**	**0.1**	**0.08**	**0.08**	**0.08**
Power consumption (A/Pin)	**5.0**	**5.0**	**6.0**	**6.0**	**6.0**	**6.0**	**6.0**
Wafer Level Burn-In							
Maximum burn-in temperature (ºC)	**175±3**	**175±3**	**175±3**	**175±3**	**175±3**	**175±3**	**175±3**
Pad Layout - Linear							
Minimum pad pitch (µm)	**65**	**50**	**50**	**50**	**50**	**50**	**50**
Minimum pad size (µm)	**50**	**40**	**40**	**40**	**40**	**40**	**40**
Maximum number of probes	**70k**	**140k**	**140k**	**140k**	**140k**	**140k**	**140k**
Pad Layout – Periphery, Area Array							
Minimum pad pitch (µm) *1	**80**	**60**	**60**	**60**	**60**	**60**	**60**
Minimum pad size (µm)	**30**	**25**	**25**	**25**	**25**	**25**	**25**
Maximum number of probes	**150k**	**300k**	**300k**	**300k**	**300k**	**300k**	**300k**
Power consumption (W/DUT – low-end microcontroller, DFT/BIST SOC *2)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Vector memory depth (M vectors – DFT/BIST SOC *2)	**64**	**128**	**128**	**128**	**256**	**256**	**256**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

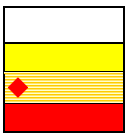


Table 32a Handler (Memory—Pick and Place) Requirements—Near-term Years UPDATED

	Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
	DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
	MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
	Parallel testing	64–128	128–256	128–256	128–256	128-256	128–256	128–256	128–512	128–512
ADD	Parallel testing – FLASH	128	256	256	512	512	1024	1024	1024	1024
	Index time (S)	3–5	3–5	2–5	2–5	2–4	2–4	2–4	2–4	2–4
	Throughput (devices per hour)	8–10K	8–10K	8–10K	8–12K	8–12K	12–20K	12–20K	12–20K	12–20K
	Sorting	5–9	5–9	5–9	5–9	5–9	5–9	5–9	5–9	5–9
	Temperature set point range (°C)	-55 to 155	-55 to 175	-55 to 175	-55 to 175	-55 to 175	-55 to 175	-55 to 175	-55 to 175	-55 to 175
	Temperature accuracy (°C)	±2	±2	±2	±2	±1.5	±1.5	±1.5	±1.5	±1.5
	Number of pins/device	40–250	40–250		6–400	40–400	6–400	40–400	6–400	6–400
	Pin pitch (mm)	0.5–1.0	0.4–1.0	0.4–1.0	0.3–1.0	0.3–1.0	0.3–1.0	0.3–1.0	0.3–1.0	0.3–1.0
	Ball edge to package edge clearance (mm)	0	0	0	0	0	0	0	0	0
	Minimum package thickness (mm)	0.3–1.8	0.3–1.8	0.3–1.8	0.2–1.8	0.2–1.8	0.2–1.8 (kitless)	0.2–1.8 (kitless)	0.2–1.8 (kitless)	0.2–1.8 (kitless)
	Conversion time (minutes)	40	1 (kitless)	1 (kitless)	1 (kitless)	1 (kitless)	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM

GEM—generic equipment model

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

Interim solutions are known

Manufacturable solutions are NOT known

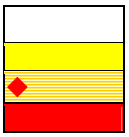
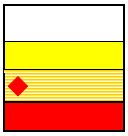


Table 32b Handler (Memory—Pick and Place) Requirements—Long-term Years UPDATED

	Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
	DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
	MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
	Parallel testing	128 - 512	128–512	128–512	128 - 512	128–512	128 - 512	128–512
ADD	Parallel testing – FLASH	1024	2048	2048	2048	2048	2048	2048
	Index time (S)	2–4	2–4	2–4	2–4	2–4	2–4	2–4
	Throughput (devices per hour)	12–20K	12–20K	12–20K	12–20K	12–20K	12–20K	12–20K
	Sorting	5–9	5–9	5–9	5–9	5–9	5–9	5–9
	Temperature set point range (°C)	-55 to 175	-55 to 175	-55 to 175	-55 to 175	-55 to 175	-55 to 175	-55 to 175
	Temperature accuracy (°C)	±1.5	±1.5	±1.5	±1.5	±1.5	±1.5	±1.5
	Number of pins/device	6–400	6–400	6–400	6–400	6–400	6–400	6–400
	Pin pitch (mm)	0.3–1.0	0.3–1.0	0.3–1.0	0.3–1.0	0.3–1.0	0.3–1.0	0.3–1.0
	Ball edge to package edge clearance (mm)	0	0	0	0	0	0	0
	Minimum package thickness (mm)	0.2–1.8 (kitless)	0.2–1.8 (kitless)	0.2–1.8 (kitless)	0.2–1.8 (kitless)	0.2–1.8 (kitless)	0.2–1.8 (kitless)	0.2–1.8 (kitless)
	Conversion time (minutes)	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM	1 (kitless) GEM–HSEM

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known



Notes for Tables 32a and b:

Index time was done from test end signal reception from tester to the test start signal transmission of handler.

Units per hour (UPH) calculated with zero-second test time and no lot-size generated interruptions.

Sort is number of stackable JEDEC tray sleeves used for output of devices.

± assumes a normal distribution centered at the temperature with 3 standard deviations equal to the ± number.

Allowable temperature rise due to a step power pulse of the corresponding power density.

Asynchronous capability is defined as the capability of the handler to input, socket and output devices independently with multiple test sites-no gang socketing.

Uninterrupted tray flow requires the handler operation to not be halted when loading/unloading trays.

Auto-Retest requires units to be retested automatically without the need for operator intervention. This is different from a simple reprobe in that the part must be socketed on a different change kit head (if possible).

Electromigration interference (EMI) event field is a measurement of electric emissions due to electrostatic discharge (ESD) events during normal handler operation.

Table 33a Handler (Logic—Pick and Place) Requirements—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Parallel testing < 10 sec test time	**8**	**16**	**16**	**16**	**16**	**32**	**16**	**32**	**64**
Parallel testing > 10 sec test time	**16**	**32**	**32**	**32**	**32**	**64**	**64**	**128**	**128**
Index time (S)	**0.3–0.4**	**0.3–0.4**	**0.25–0.3**	**0.25–0.3**	**0.25**	**0.25**	**0.25**	**0.25**	**0.25**
Throughput (devices per hour)	**8–12K**	**8–12K**	**9–14K**	**9–14K**	**12–20K**	**12–20K**	**12–20K**	**12–20K**	**12–20K**
Sorting	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**
Temperature set point range (ºC)	**-55 to 155**	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**
Tj accuracy at start of test (ºC)	**± 0.5**	**± 2**	**± 2**	**± 2**	**± 2**	**± 2**	**± 2**	**± 2**	**± 2**
Total thermal load (Watts) – MPU	**125**	**125**	**150**	**150**	**175**	**200**	**200**	**200**	**200**
Thermal Watt density (Watts/cm^2) – MPU	**130**	**130**	**175**	**175**	**200**	**225**	**225**	**225**	**225**
Maximum socket load per unit (kg)	**24**	**27**	**50**	**50**	**35**	**60**	**35**	**60**	**60**
Asynchronous capability	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Number of pins or lands/device	**750**	**750**	**800**	**800**	**850**	**850**	**850**	**850**	**850**
Pin/land pitch (mm)	**1.1**	**1.1**	**0.3**	**0.3**	**0.8**	**0.3**	**0.3**	**0.3**	**0.2**
Conversion time (minutes)	**30**	**30**	**15**	**15**	**15**	**5**	**5**	**5**	**5**
Uninterrupted tray loading/auto-2A	**No**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Reliability (hours)	**400**	**600**	**800**	**1000**	**1000**	**1000**	**1000**	**1200**	**1200**

Table 33b Handler (Logic—Pick and Place) Requirements—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Parallel testing < 10 sec test time	**64**	**64**	**64**	**64**	**64**	**64**	**64**
Parallel testing > 10 sec test time	**128**	**128**	**128**	**128**	**256**	**256**	**256**
Index time (S)	**0.25**	**0.25**	**0.25**	**0.25**	**0.25**	**0.25**	**0.25**
Throughput (devices per hour)	**12–20K**	**20–28K**	**20–28K**	**20–28K**	**20–28K**	**20–28K**	**20–28K**
Sorting	**3–6**	**3–6**	**3–6**	**3–6**	**3–6**	**3-6**	**3–6**
Temperature set point range (ºC)	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**	**-55 to 175**
Tj accuracy at start of test (ºC)	**± 2**	**± 2**	**± 2**	**± 2**	**± 2**	**± 2**	**± 2**
Total thermal load (Watts) – MPU	**200**	**250**	**250**	**250**	**300**	**300**	**300**
Thermal Watt density (Watts/cm^2) – MPU	**225**	**250**	**250**	**250**	**250**	**250**	**250**
Maximum socket load per unit (kg)	**60**	**65**	**65**	**65**	**75**	**75**	**75**
Asynchronous capability	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Number of pins or lands/device	**850**	**900**	**900**	**900**	**1000**	**1000**	**1000**
Pin/land pitch (mm)	**0.3**	**0.2**	**0.2**	**0.3**	**0.2**	**0.2**	**0.2**
Conversion time (minutes)	**5**	**5**	**5**	**5**	**5**	**5**	**5**
Uninterrupted tray loading/auto-2A	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
Reliability (hours)	**1000**	**1200**	**1400**	**1400**	**1400**	**1400**	**1400**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

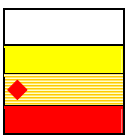


Table 34a Handler (Network and Communications—Pick and Place)—Near-term Years

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Parallel testing	4	8	8	8	8	8	16	16	16
Index time (S)	0.3–0.4	0.3–0.4	0.3–0.4	0.3–0.4	0.25–0.3	0.25–0.3	0.25	0.25	0.25
Throughput (devices per hour)	4–6K	8–12K	8–12K	8–12K	9–14K	9–14K	12–20K	12–20K	12–20K
Sorting	3–6	3–6	3–6	3–6	3–6	3–6	3–6	3–6	3–6
Set point range (ºC)	-45 to +150	-45 to +150	-45 to +150	-45 to +150	-45 to +150	-45 to +150	-45 to +150	-45 to +150	-45 to +150
Temperature accuracy (ºC)	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5
Allowable device temperature rise (ºC)	20	20	20	20	20	20	20	20	20
Maximum socket load per unit (kg)	16	20	24	27	30	30	35	35	35
Asynchronous capability	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Number of pins or lands/device	700	700	750	750	800	800	850	850	850
Pin/land pitch (mm)	1.2	1.2	1.1	1.1	1	1	0.8	0.6	0.6
Conversion time (minutes)	30	30	30	30	15	15	15	5	5
Uninterrupted tray loading/auto-2A	No	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Reliability (hours)	80	100	100	168	168	500	500	1000	1000

Table 34b Handler (Network and Communications—Pick and Place)—Long-term Years

Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Parallel testing	16	16	16	32	32	32	32
Index time (S)	0.25	0.25	0.25	0.25	0.25	0.25	0.25
Throughput (devices per hour)	12–20K	12–20K	12–20K	20–28K	20–28K	20–28K	20–28K
Sorting	3–6	3–6	3–6	3–6	3–6	3–6	3–6
Set point range (ºC)	-45 to +150	-45 to +150	-45 to +150	-45 to +150	-45 to +150	-45 to +150	-45 to +150
Temperature accuracy (ºC)	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5	-0.5
Allowable device temperature rise (ºC)	20	20	20	20	20	20	20
Maximum socket load per unit (kg)	35	35	35	35	35	35	35
Asynchronous capability	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Number of pins or lands/device	850	850	850	900	900	900	1000
Pin/land pitch (mm)	0.6	0.6	0.6	0.4	0.4	0.4	0.4
Conversion time (minutes)	5	5	5	5	5	5	5
Uninterrupted tray loading/auto-2A	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Reliability (hours)	1000	1000	1000	1000	1000	1000	1000

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

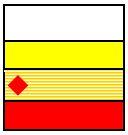


Table 35a Prober (Logic MPU—Pick and Place) Requirements—Near-term Years

Year of Production		*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm)		*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)		*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Printed Gate Length (nm)		*45*	*40*	*35*	*32*	*28*	*25*	*22*	*20*	*18*
MPU Physical Gate Length (nm)		*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
Wafer diameter (mm)		**300**	**300**	**300**	**300**	**300**	**300**	**300**	**300**	**300**
Pad pitch	Peripheral (mm)	**40–100**	**40–100**	**40–100**	**30–80**	**30–80**	**30–60**	**30–60**	**30–60**	**30–60**
	Bump (mm)	**30**	**30**	**30**	**30**	**30**	**20**	**20**	**20**	**20**
Wafer thickness (mm)		**80–775**	**80–775**	**80–775**	**80–775**	**80–775**	**50–1000**	**50–1000**	**50–1000**	**50–1000**
Maximum I/O pads		**3000**	**3000**	**3000**	**4000**	**4000**	**5300**	**5300**	**5300**	**5300**
Chuck positioning accuracy	X & Y (µm)	**4**	**4**	**4**	**2**	**2**	**2**	**2**	**2**	**2**
	Z (µm)	**2**	**2**	**1**	**1**	**1**	**0.5**	**0.5**	**0.5**	**0.5**
Probe-to-pad alignment (µm)		**4.5**	**4.5**	**4.5**	**4.5**	**4.5**	**3.5**	**3.5**	**3.5**	**3.5**
Maximum chuck force (kg)		**50**	**100**	**100**	**100**	**100**	**100**	**100**	**100**	**100**
Parallel testing		**16**	**32**	**32**	**32**	**32**	**64**	**64**	**64**	**128**
Set point range (ºC)		**-30 to +85**	**-30 to +85**	**-30 to +85**	**-30 to +85**	**-30 to +85**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**
Total power (Watts)		**150**	**150**	**200**	**200**	**250**	**250**	**250**	**250**	**250**
Power density (Watt/cm^2)		**90**	**90**	**90**	**90**	**120**	**120**	**120**	**120**	**120**

Table 35b Prober (Logic MPU—Pick and Place) Requirements—Long-term Years

Year of Production		*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm)		*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)		*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Printed Gate Length (nm)		*16*	*14*	*13*	*11*	*10*		
MPU Physical Gate Length (nm)		*11*	*10*	*9*	*8*	*7*	*6*	*6*
Wafer diameter (mm)		**450**	**450**	**450**	**450**	**450**	**450**	**450**
Pad pitch	Peripheral (mm)	**30–60**	**30–60**	**30–60**	**30–60**	**30–60**	**30–60**	**3–60**
	Bump (mm)	**20**	**20**	**20**	**20**	**20**	**20**	**20**
Wafer thickness (mm)		**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**	**50–1000**
Maximum I/O pads		**5300**	**5300**	**5300**	**5300**	**5300**	**5300**	**5300**
Chuck positioning accuracy	X & Y (µm)	**2**	**2**	**2**	**2**	**2**	**2**	**2**
	Z (µm)	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**	**0.5**
Probe-to-pad alignment (µm)		**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**	**3.5**
Maximum chuck force (kg)		**100**	**100**	**100**	**100**	**100**	**100**	**100**
Parallel testing		**128**	**128**	**128**	**128**	**128**	**128**	**128**
Set point range (ºC)		**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**	**-45 to +125**
Total power (Watts)		**250**	**300**	**300**	**250**	**300**	**300**	**300**
Power density (Watt/cm^2)		**120**	**120**	**120**	**120**	**120**	**120**	**120**

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

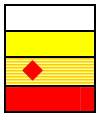


Table 36 Test Handler and Prober Difficult Challenges UPDATED

		CHALLENGE	ISSUE / GOAL
IS	Memory handler	Package form factors	Variety of sizes, thicknesses, and ball pitches requires kitless handlers with thin-die handling capability
		Ball-to-package edge gap	As this decreases from 0.6 mm to 0 mm, new handling and socketing methods must be introduced
		Massive parallelism	**Parallelism at greater than x128 drives** roadmap, thermal, and alignment challenges
	Logic handler	Thermal control	Improved temperature control and temperature rise control due to high power densities during test
		Operations improvements	Continuous lot processing (lot cascading), auto-retest, asynchronous device socketing, low-conversion times
		ESD	Products more sensitive to ESD, while on-die protection circuitry increases cost.
		Packaging technology	Lower stress socketing, low-cost change kits, higher I/O count, heat lids change thermal characteristics
		Through put and multi-site	Increase in multi-site handling capability for short test time devices (1–7 seconds), thus increase in throughput
	Netcom handler	New packaging technologies	Known good die solutions (KGD), stacked die packaging, thin die packaging
		Temperature control	Wide range tri-temperature soak requirements (-45ºC to 150ºC) increases system complexity
		Operations improvements	Continuous lot processing (lot cascading), auto-retest, low conversion times, asynchronous operation
		EMI/RF up to 40 GHz	Shielding issues associated with high frequency testing (>10 GHz)
	Logic prober	Thermal contact resistance between wafer and chuck	The high thermal resistance and variation in contact resistance across chuck are required to improve temperature control and reduce temperature rise of device under test
		Heat dissipation at elevated temperature	Heat dissipation of >100 Watts at > 85ºC is a configuration gap in the prober industry
		Probe card optical standardization	With advancement in probe card technology a new optical alignment methodology must be developed

Table 37 Probe Card Difficult Challenges—Near-term Years

CHALLENGE	*ISSUE / GOAL*
Geometry	Probe technologies to support peripheral fine pitch probe of 25 μm, peripheral staggered pad probes at effective pitches of 20/40, and fine pitch (45 μm) for dual row, non-staggered probing on all four die sides. Fine pitch vertical probe technologies to support 130 μm pitch area array solder bump and 50 μm pitch staggered pad devices. Multi-site pad probing technologies with corner pitch capability below 125 μm. Reduction of pad damage at probe commensurate with pad size reductions (or better). Alternative probe technology for 75 μm on 150 μm pitch dense array (vertical probe; bumped device). Increasing probe array planarity requirements in combination with increasing array size.
Parallel test	Need a probe technology to handle the complexity of SOC devices while probing more than one device. Current probe technologies have I/O limitations for bumped device probes.
Probing at temperature	Reduce effects on probes for non-ambient testing -40 to 150°C; especially for fine-pitch devices. For effects on Handlers and Probers, see that section.
Product	Probe technologies to direct probe on copper bond pads including various oxidation considerations. Probe technologies for probing over active circuitry (including flip-chip).
Probe force	Reduce per pin force required for good contact resistance to lower total load for high pin count and multi DUT probe applications. Evaluation and reduction of probe force requirements to eliminate die damage, including interlayer dielectric damage with low-κ dielectrics.
Probe cleaning	Development of high temperature (85 C–15°C) *in situ* cleaning mediums/methods, particularly for fine pitch, multi-DUT and non-traditional probes. Reduction of cleaning requirements while maintaining electrical performance to increase lifetime.
Cost and delivery	Fine pitch or high pin count probe cards are too expensive and take too long to build. Time and cost to repair fine pitch or high pin count probe cards is very high. The time between chip design completion (“tape-out”) and the availability of wafers to be probed is less than the time required to design and build a probe card in almost every probe technology except traditional cantilever. Space transformer lead times are too long, thus causing some vertical probe technologies to have lengthy lead-times.
Probe metrology	Tools are required that support fine pitch probe characterization and pad damage measurements. Metrology correlation is needed—repair versus on-floor usage.
High power devices	Probe technologies will need to incorporate thermal management features capable of handling device power dissipations approaching 1000 Watts and the higher currents (>= 1.5 amp) flowing through individual probe points.
Contact resistance	Probe technologies that achieve contact resistance <.5 Ohms initially and throughout use are needed.
High frequency probing	Traditional probe technologies do not have the necessary electrical bandwidth for higher frequency devices. At the top end are RF devices, requiring up to 40 GHz.

Table 38a Wafer Probe Technology Requirements—Near-term Years UPDATED

	Year of Production	2005		2006		2007		2008		2009		2010		2011		2012		2013	
	DRAM ½ Pitch (nm) (contacted)	80		70		65		57		50		45		40		36		32	
	I/O Pad Size (µm)	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
	Wirebond	35	60	30	55	30	55	25	45	25	45	25	45	25	45	20	35	20	35
	Bump	75	75	75	75	60	60	60	60	50	50	50	50	50	50	50	50	50	50
	Scrub (% of I/O)	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH
	Wirebond	25	50	25	50	25	50	20	40	20	40	20	40	20	40	20	40	20	40
	Bump	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30
	Multi-DUT Volume (% of Total Product Type Wafers Probed)																		
	Memory (DRAM)	99.9		99.9		99.9		99.9		99.9		99.9		99.9		99.9		99.9	
	ASIC	50		60		75		75		75		75		75		75		75	
	Microprocessor	50		60		75		75		75		75		75		75		85	
	RF	45		50		50		60		60		60		60		60		60	
	Mixed-signal	60		60		75		75		80		80		80		80		80	
	Size of Probed Area (mm^2)																		
	Memory (DRAM)	50% of wafer		50% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer	
ADD	Memory (FLASH)	50% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer	
	ASIC	2050		2050		2050		2400		2400		2400		2400		2400		2400	
	Microprocessor	2050		2050		2050		2400		2400		2400		2400		2400		2400	
	RF	900		900		1225		1225		1225		1225		1225		1225		1225	
	Mixed-signal	1413		1413		1600		1600		1600		1600		1600		1600		1600	
	Number of Probe Points /Touchdown	Signal	Total	Signal	Total	Signal	Total	Signal	Total	Signal	Total	Signal	Total	Signal	Total	Signal	Total	Signal	Total
	Memory (DRAM)	14500	18700	14500	18700	17000	20000	17000	20000	17000	20000	17000	20000	17000	20000	20000	25000	20000	25000
	ASIC	1050	4000	1050	5000	1050	5000	1200	6000	1500	7500	1500	7500	1500	7500	3000	9000	3000	9000
	Microprocessor	1024	10000	1024	15000	1024	20000	1024	20000	1024	20000	1024	20000	1024	20000	2000	30000	2000	30000
	RF	250	450	250	450	350	630	350	630	350	630	350	630	350	630	350	630	350	630
	Mixed-signal	450	600	450	600	510	680	510	680	510	680	510	680	510	680	510	680	510	680
	Maximum Current (mA)	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage
	Memory (DRAM)	100	<10	125	<10	125	<10	125	<10	125	<10	125	<10	125	<10	125	<10	125	<10
	ASIC	200	<10	300	<10	400	<10	500	<10	500	<10	500	<10	500	<10	1000	<10	1000	<10
	Microprocessor	800	<10	1000	<10	1200	<10	1200	<10	1500	<10	1500	<10	1500	<10	1500	<10	1500	<10

	Year of Production	*2005*		*2006*		*2007*		*2008*		*2009*		*2010*		*2011*		*2012*		*2013*	
	DRAM ½ Pitch (nm) (contacted)	*80*		*70*		*65*		*57*		*50*		*45*		*40*		*36*		*32*	
	RF	**200**	**<10**	**225**	**<10**	**225**	**<10**	**225**	**<10**	**225**	**<10**	**225**	**<10**	**225**	**<10**	**225**	**<10**	**225**	**<10**
	Mixed-signal	**250**	**<10**	**275**	**<10**	**275**	**<10**	**275**	**<10**	**275**	**<10**	**275**	**<10**	**275**	**<10**	**275**	**<10**	**275**	**<10**
	Maximum Resistance (Ohm)	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**	**Contact**	**Series**
	Memory (DRAM)	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**
	ASIC	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**	**<0.5**	**<3**
	Microprocessor	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**	**<0.5**	**<2**
	RF	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**
	Mixed-signal	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**	**<0.5**	**<1.5**
	Chuck Set-point (°C)	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
	Memory (DRAM)	**-40**	**140**	**-40**	**150**	**-40**	**150**	**-50**	**180**	**-50**	**180**	**-50**	**180**	**-50**	**180**	**-50**	**180**	**-50**	**180**
	ASIC	**25**	**110**	**0**	**140**	**0**	**140**	**-10**	**140**	**-10**	**140**	**-10**	**140**	**-10**	**14**	**-10**	**14**	**-10**	**14**
	Microprocessor	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**	**-30**	**135**
	RF	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**	**5**	**120**
	Mixed-signal	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**	**25**	**125**
	Soak Time (minutes)																		
	Memory (DRAM)	**10**		**8**		**8**		**8**		**7**		**7**		**7**		**7**		**7**	
	ASIC	**8**		**7**		**7**		**7**		**6**		**6**		**6**		**6**		**6**	
	Microprocessor	**10**		**10**		**10**		**9**		**9**		**9**		**9**		**9**		**9**	
	RF	**10**		**10**		**9**		**9**		**9**		**9**		**9**		**9**		**9**	
	Mixed-signal	**10**		**10**		**9**		**9**		**9**		**9**		**9**		**9**		**9**	
	Order Lead-time—Single DUT (weeks)	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**
	Memory (DRAM)	**6**	**3**	**5.5**	**3**	**5**	**3**	**4**	**2**	**4**	**2**	**4**	**2**	**4**	**2**	**4**	**2**	**4**	**2**
	ASIC	**2.5**	**1.5**	**2.5**	**1.5**	**2.5**	**1.5**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**
	Microprocessor	**2.5**	**1.5**	**2.5**	**1.5**	**2.5**	**1.5**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**
	RF	**4**	**2**	**3.5**	**1.5**	**3.5**	**1.5**	**3**	**1**	**3**	**1**	**3**	**1**	**3**	**1**	**3**	**1**	**3**	**1**
	Mixed-signal	**3**	**2**	**2.5**	**1.5**	**2.5**	**1.5**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**	**2**	**1**
	Order Lead-time—Multi-DUT (weeks)	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**	**1st Order**	**Re-Order**
	Memory DRAM)	**7**	**4**	**6**	**3**	**5**	**3**	**4.5**	**2.5**	**4.5**	**2.5**	**4.5**	**2.5**	**4.5**	**2.5**	**4.5**	**2.5**	**4.5**	**2.5**
	ASIC	**5**	**2**	**4**	**1.5**	**3.5**	**1.5**	**3**	**1**	**3**	**1**	**3**	**1**	**3**	**1**	**3**	**1**	**3**	**1**

	Year of Production	*2005*		*2006*		*2007*		*2008*		*2009*		*2010*		*2011*		*2012*		*2013*	
	DRAM ½ Pitch (nm) (contacted)	*80*		*70*		*65*		*57*		*50*		*45*		*40*		*36*		*32*	
	Microprocessor	4	2	4	1.5	3.5	1.5	3	1	3	1	3	1	3	1	3	1	3	1
	RF	5	3	4.5	2	4	1.5	4	1	4	1	4	1	4	1	4	1	4	1
	Mixed-signal	4	2	3.5	2	3	1.5	3	1	3	1	3	1	3	1	3	1	3	1
	Touchdowns Before Clean (Cantilever)	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline
	Memory (DRAM)	400	20,000	400	20,000	450	20,000	450	20,000	450	20,000	450	20,000	450	20,000	450	20,000	450	20,000
	ASIC	3,250	60,000	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000
	Microprocessor	1,250	50,000	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000
	RF	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000
	Mixed-signal	2,000	200,000	2,000	200,000	2,000	300,000	2,000	300,000	2,000	300,000	2,000	300,000	2,000	300,000	2,000	300,000	2,000	300,000
	Touchdowns Before Clean (Vertical)	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline
	Memory (DRAM)	1,500	20,000	2,000	25,000	2,000	25,000	2,000	25,000	2,000	25,000	2,000	25,000	2,500	27,500	2,500	27,500	2,500	27,500
	ASIC	1,500	17,500	2,000	20,000	2,000	20,000	2,000	20,000	2,000	20,000	2,000	20,00	2,500	22,500	2,500	22,500	2,500	22,500
	Microprocessor	1,500	80,000	2,000	100,000	2,000	100,000	2,000	100,000	2,000	100,000	2,000	100,000	2,500	100,000	2,500	100,000	2,500	100,000
	RF	100	20,000	100	25,000	100	25,000	125	25,000	125	25,000	125	25,000	125	27,500	125	27,500	125	27,500
	Mixed-signal	1,500	85,000	2,000	87,500	2,000	87,500	2,000	87,500	2,000	87,500	2,000	87,500	2,500	90,000	2,500	90,000	2,500	90,000

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known

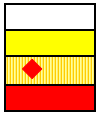


Table 38b Wafer Probe Technology Requirements—Long-term Years UPDATED

	Year of Production	2014		2015		2016		2017		2018		2019		2020	
	DRAM ½ Pitch (nm) (contacted)	28		25		22		20		18		16		14	
	I/O Pad Size (µm)	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
	Wirebond	20	35	15	25	15	25	15	25	15	25	15	25	15	25
	Bump	50	50	50	50	50	50	50	50	50	50	50	50	50	50
	Scrub (% of I/O)	Offline	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH
	Wirebond	20	40	20	40	20	40	20	40	20	40	20	40	20	40
	Bump	30	30	30	30	30	30	30	30	30	30	30	30	30	30
	Multi-DUT Volume (% of Total Product Type Wafers Probed)														
	Memory (DRAM)	99.9		99.9		99.9		99.9		99.9		99.9		99.9	
	ASIC	75		75		75		75		75		75		75	
	Microprocessor	85		85		85		85		85		85		85	
	RF	60		80		60		60		60		60		60	
	Mixed-signal	80		80		80		80		80		80		80	
	Size of Probed Area (mm^2)														
	Memory (DRAM)	100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer	
ADD	Memory (FLASH)	100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer		100% of wafer	
	ASIC	2400		2400		2400		2400		2400		2400		2400	
	Microprocessor	2400		2400		2400		2400		2400		2400		2400	
	RF	1225		1225		1225		1225		1225		1225		1225	
	Mixed-signal	1600		1600		1600		1600		1600		1600		1600	
	Number of Probe Points /Touchdown	Signal	Total	Signal	Total	Signal	Total	Signal	Total	Signal	Total	Signal	Total	Signal	Total
	Memory (DRAM)	20000	25000	20000	25000	20000	25000	20000	25000	20000	25000	20000	25000	20000	25000
	ASIC	3000	9000	3000	9000	3000	9000	3000	9000	3000	9000	3000	9000	3000	9000
	Microprocessor	2000	30000	2000	30000	2000	30000	2000	30000	30000	6000	30000	6000	30000	6000
	RF	350	630	350	630	350	630	350	630	350	630	350	630	350	630
	Mixed-signal	510	680	510	680	510	680	510	680	510	680	510	680	510	680
	Maximum Current (mA)	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage	Probe Tip	DC Leakage
	Memory (DRAM)	125	<10	125	<10	125	<10	125	<10	125	<10	125	<10	125	<10
	ASIC	1000	<10	1000	<10	1000	<10	1000	<10	1000	<10	1000	<10	1000	<10
	Microprocessor	1500	<10	1500	<10	1500	<10	1500	<10	1500	<10	1500	<10	1500	<10
	RF	225	<10	225	<10	225	<10	225	<10	225	<10	225	<10	225	<10
	Mixed-signal	275	<10	275	<10	275	<10	275	<10	275	<10	275	<10	275	<10
	Maximum Resistance (Ohm)	Contact	Series	Contact	Series	Contact	Series	Contact	Series	Contact	Series	Contact	Series	Contact	Series
	Memory (DRAM)	<0.5	<3	<0.5	<3	<0.5	<3	<0.5	<3	<0.5	<3	<0.5	<3	<0.5	<3
	ASIC	<0.5	<3	<0.5	<3	<0.5	<3	<0.5	<3	<0.5	<3	<0.5	<3	<0.5	<3
	Microprocessor	<0.5	<2	<0.5	<2	<0.5	<2	<0.5	<2	<0.5	<2	<0.5	<2	<0.5	<2

	Year of Production	2014		2015		2016		2017		2018		2019		2020	
	DRAM ½ Pitch (nm) (contacted)	28		25		22		20		18		16		14	
	RF	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5
	Mixed-signal	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5	<0.5	<1.5
	Chuck Set-point (°C)	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
	Memory (DRAM)	-50	180	-50	180	-50	180	-50	180	-50	180	-50	180	-50	180
	ASIC	-10	14	-10	14	-10	14	-10	14	-10	14	-10	14	-10	14
	Microprocessor	-30	135	-30	135	-30	135	-30	135	-30	135	-30	135	-30	135
	RF	5	120	5	120	5	120	5	120	5	120	5	120	5	120
	Mixed-signal	25	125	25	125	25	125	25	125	25	125	25	125	25	125
	Soak Time (minutes)														
	Memory (DRAM)	7		7		7		7		7		7		7	
	ASIC	6		6		6		6		6		6		6	
	Microprocessor	9		9		9		9		9		9		9	
	RF	9		9		9		9		9		9		9	
	Mixed-signal	9		9		9		9		9		9		9	
	Order Lead-time—Single DUT (weeks)	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order
	Memory (DRAM)	4	2	4	2	4	2	4	2	4	2	4	2	4	2
	ASIC	2	1	2	1	2	1	2	1	2	1	2	1	2	1
	Microprocessor	2	1	2	1	2	1	2	1	2	1	2	1	2	1
	RF	3	1	3	1	3	1	3	1	3	1	3	1	3	1
	Mixed-signal	2	1	2	1	2	1	2	1	2	1	2	1	2	1
	Order Lead-time—Multi-DUT (weeks)	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order	1st Order	Re-Order
	Memory DRAM)	4.5	2.5	4.5	2.5	4.5	2.5	4.5	2.5	4.5	2.5	4.5	2.5	4.5	2.5
	ASIC	3	1	3	1	3	1	3	1	3	1	3	1	3	1
	Microprocessor	3	1	3	1	3	1	3	1	3	1	3	1	3	1
	RF	4	1	4	1	4	1	4	1	4	1	4	1	4	1
	Mixed-signal	3	1	3	1	3	1	3	1	3	1	3	1	3	1
	Touchdowns Before Clean (Cantilever)	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline
	Memory (DRAM)	450	20,000	450	20,000	450	20,000	450	20,000	450	20,000	450	20,000	450	20,000
	ASIC	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000	3,500	60,000
	Microprocessor	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000	1,500	50,000
	RF	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000	1,000	100,000
	Mixed-signal	2,000	300,000	2,000	300,000	2,000	300,000	2,000	300,000	2,000	300,000	2,000	300,000	2,000	300,000
	Touchdowns Before Clean (Vertical)	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline	Online	Offline
	Memory (DRAM)	2,500	27,500	2,500	27,500	2,500	27,500	2,500	27,500	2,500	27,500	2,500	27,500	2,500	27,500
	ASIC	2,500	22,500	2,500	22,500	2,500	22,500	2,500	22,500	2,500	22,500	2,500	22,500	2,500	22,500

32 Test and Test Equipment

	Year of Production	*2014*		*2015*		*2016*		*2017*		*2018*		*2019*		*2020*	
	DRAM ½ Pitch (nm) (contacted)	*28*		*25*		*22*		*20*		*18*		*16*		*14*	
	Microprocessor	2,500	100,000	2,500	100,000	2,500	100,000	2,500	100,000	2,500	100,000	2,500	100,000	2,500	100,000
	RF	125	27,500	125	27,500	125	27,500	125	27,500	125	27,500	125	27,500	125	27,500
	Mixed-signal	2,500	90,000	2,500	90,000	2,500	90,000	2,500	90,000	2,500	90,000	2,500	90,000	2,500	90,000

Manufacturable solutions exist, and are being optimized
Manufacturable solutions are known
Interim solutions are known
Manufacturable solutions are NOT known