Yield Enhancement - International Technical Working Group

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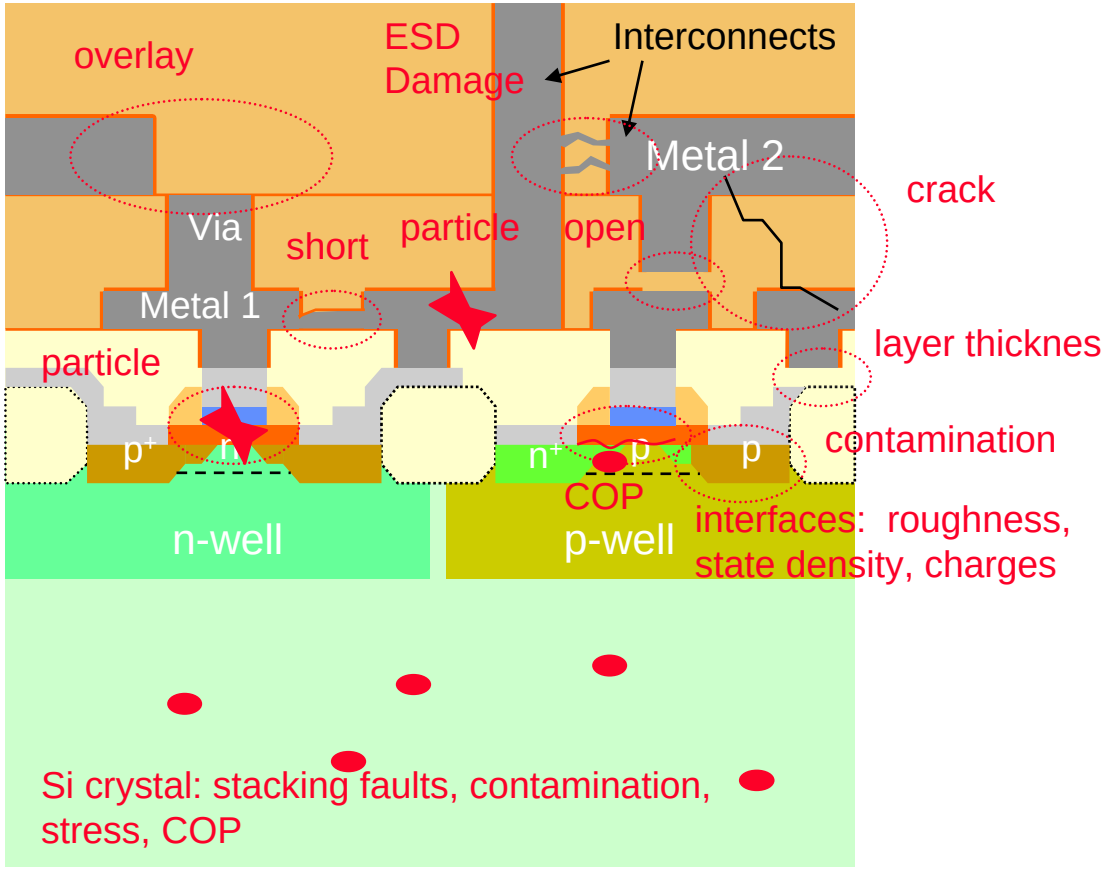
Outline

- Examples for Yield Loss
- Chapter Outline
- Organization of the Chapter
- 2008 Key Challenges (updated)
- Contributors
- Subchapters
  - Defect Detection and Characterization
  - Wafer Environment Contamination Control
  - Yield Model and Defect Budgets
- Outlook

Examples for Yield Loss

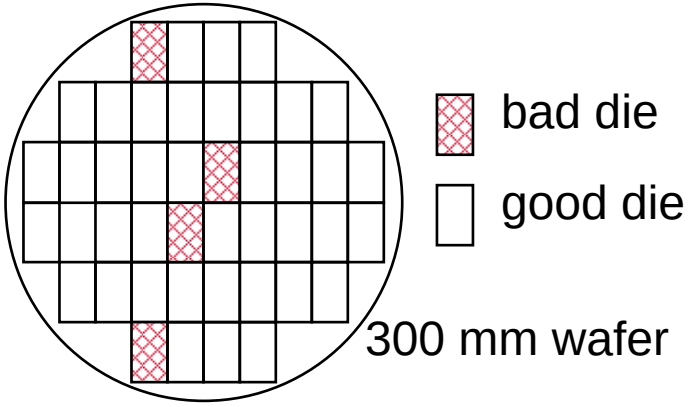


- processes: implantation, etching, deposition, planarization, cleaning,…
- faults and problems: contamination, particles, defects, overlay faults, cracks, roughness, stress

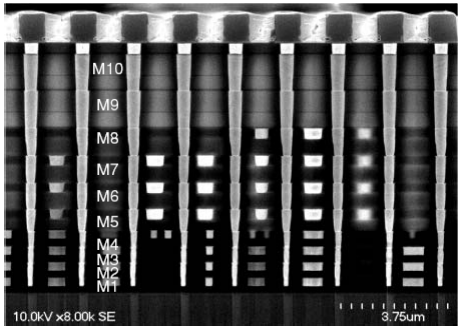
Chapter Outline

- Scope and topics
  - improvement from R&D yield level to mature yield
  - limited to front-end processing
  - defect detection and characterization
  - yield learning/fast ramp

$$\text{Yield} = \frac{\text{good die}}{\text{good die} + \text{bad die}}$$



Gordon Moore: "There is no fundamental obstacle to achieving device yields of 100%." (Electronics, 38 (8), 1965)



Takayuki Ohba, 21 FUJITSU Sci. Tech. J., 38,1,(June 2002): Cross-sectional SEM picture of 10-level Cu dual-Damascene structure fabricated using SiLK™ at the lower level (minimum feature size from M1 to M4) of multilevel interconnects.

Organization of the Chapter

- **Chair:** Lothar Pfitzner (Fraunhofer IISB)
  Co-Chair: Dilip Patel (Intel)

- Difficult Challenges
  - Table YE2
- Technology Requirements and Potential Solutions
  - Yield Model and Defect Budget (YMDB)
    - Chair: Sumio Kuwabara (NEC) - Japan
    - Table YE3, YE4, YE5
  - Defect Detection and Characterization (DDC)
    - Chair: Ines Thurner (Qimonda) - Europe
    - Table YE6, YE7, YE8
  - Wafer Environment Contamination Control (WECC) – USA
    - Chair: Kevin Pate (Intel) – USA,
      Andreas Neuber (MW - Zander)-Europe
    - Table YE9

2008 YE ITWG Contributors

Europe

Ines Thurner (DDC; Qimonda)
Lothar Pfitzner (Chair; Fraunhofer IISB)
Andreas Nutsch (DDC; Fraunhofer IISB)
Andreas Neuber (WECC; M+W Zander)
Benoit Hirschberger (DDC; ST)
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Michael Otto (WECC; Fraunhofer IISB)
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Thank you very much!

United States

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Stephen Toebes (WECC; Brooks)
Steve Hues (WECC; Micron Technology)
Terry Stange (WECC; Hach Ultra)
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William Moore (WECC; IBM)
James S. Clarke (DDC; Intel)
Kevin Sequin (WECC; Donaldson)

Update: 2008 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- ***Near Term (>22 nm)***
  - ***Detection of Multiple Killer Defect Types / Signal to Noise Ratio –*** Detection of multiple killer defect types and their simultaneous differentiation at high capture rates, low cost of ownership and high throughput. It is a challenge to find small but yield relevant defects under a vast amount of nuisance and false defects.
  - ***3D Inspection –*** For inspection tools the capability to inspect high aspect ratios but also to detect non-visuals such as voids, embedded defects, and sub-surface defects is crucial. The demand for high-speed and cost-effective inspection tools remains. The need for high-speed and cost-effective 3D inspection tools becomes crucial as the importance of 3D defect types increases. E-beam inspection seems not to be the solution for all those tasks any more.
  - ***Process Stability vs. Absolute Contamination Level Including the Correlation to Yield*** Test structures, methods and data are needed for correlating defects caused by wafer environment and handling with yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.
  - ***Wafer Edge and Bevel Monitoring and Contamination Control –*** Defects and process problems around wafer edge and wafer bevel are identified to cause yield problems. Currently, the monitoring and contamination control methods require intensive development.

Update: 2008 Key Challenges

The Yield Enhancement community is challenged by the following topics:

- ***Long Term (<22 nm)***
  - ***Non-Visual Defects and Process Variations:*** Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes. The irregularity of features in logic areas makes them very sensitive to systematic yield loss mechanisms such as patterning process variations across the lithographic process window.

  - ***In - line Defect Characterization and Analysis –*** Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality.

  - ***Development of model-based design-manufacturing interface —*** Due to Optical Proximity Correction (OPC) and the high complexity of integration, the models must comprehend greater parametric sensitivities, ultra-thin film integrity, impact of circuit design, greater transistor packing, etc.

Yield Model and Defect Budget

- 2008 Key Message
  - solution required to get updated data of PWP data or control limits through IDMs
  - Cooperation from ISMI required
- 2008 Update
  - Update of the numbers – adjust to Flash requirements
  - Critical review of the according key challenges
- Outlook
  - Future of the DB needs new structure

Outlook: Roadmap for Systematic Yield Loss Issues

- New sub-chapter proposed for 2009 Revision
- Outline:
  - **Definitions**
  - **Tables showing a roadmap for**
    - **for necessary methodology and diagnostic systems**
    - **For identification of non-visual defects and process variations**
  - **Key Challenge and Potential solutions**
    - **Definition and wording for 2008 update**
    - **Wording and outline potential solutions**

Defect Detection and Characterization

- 2008 update
  - Adaption of the DDC specific key challenges
  - finalize of Flash as design rule driver: Conversion of tables to Flash requirements (Flash has the most advanced technology and is therefore the driver)
  - Update tool capabilities
  - Specification of defect coordinate accuracy for bevel inspection tools
  - Defect detection and characterization (DDC) alignment with Litho, FEP requirements
- future objectives
  - Challenge in identification and yield impact of systematic non-visual defects
  - Evaluate the need of flatness and nano-topography inspection
  - Specification for bevel monitoring
  - Contamination level of inspection tools

Wafer Contamination and Environment Control

Focus items (Ultrapure Water, Chemicals, Gas, Airborne/Surface Molecular Contamination)

- Particles: Measurement, composition, critical size, identify yield correlation, deposition model
- Organics: Measurement, speciation, identify yield correlation, deposition model
- Ions and molecular contamination: Deposition model
- CVD/ALD precursor contamination control requirements
- Airborne Molecular Contamination integrated control concept, metrology requirements

Outlook

Development/ Improvement of the Yield Enhancement chapter

- DDC – WECC study: Impact of particles on yield
- Reflection of current status and future requirements needs subsequent adjustment of outline and content of the chapter
- Request to IDMs, JEITA, ISMI, academia contributing to ITRS:
  - assure that sufficient contributors and resources are available
  - surveys required for future updates e.g. DB&YM